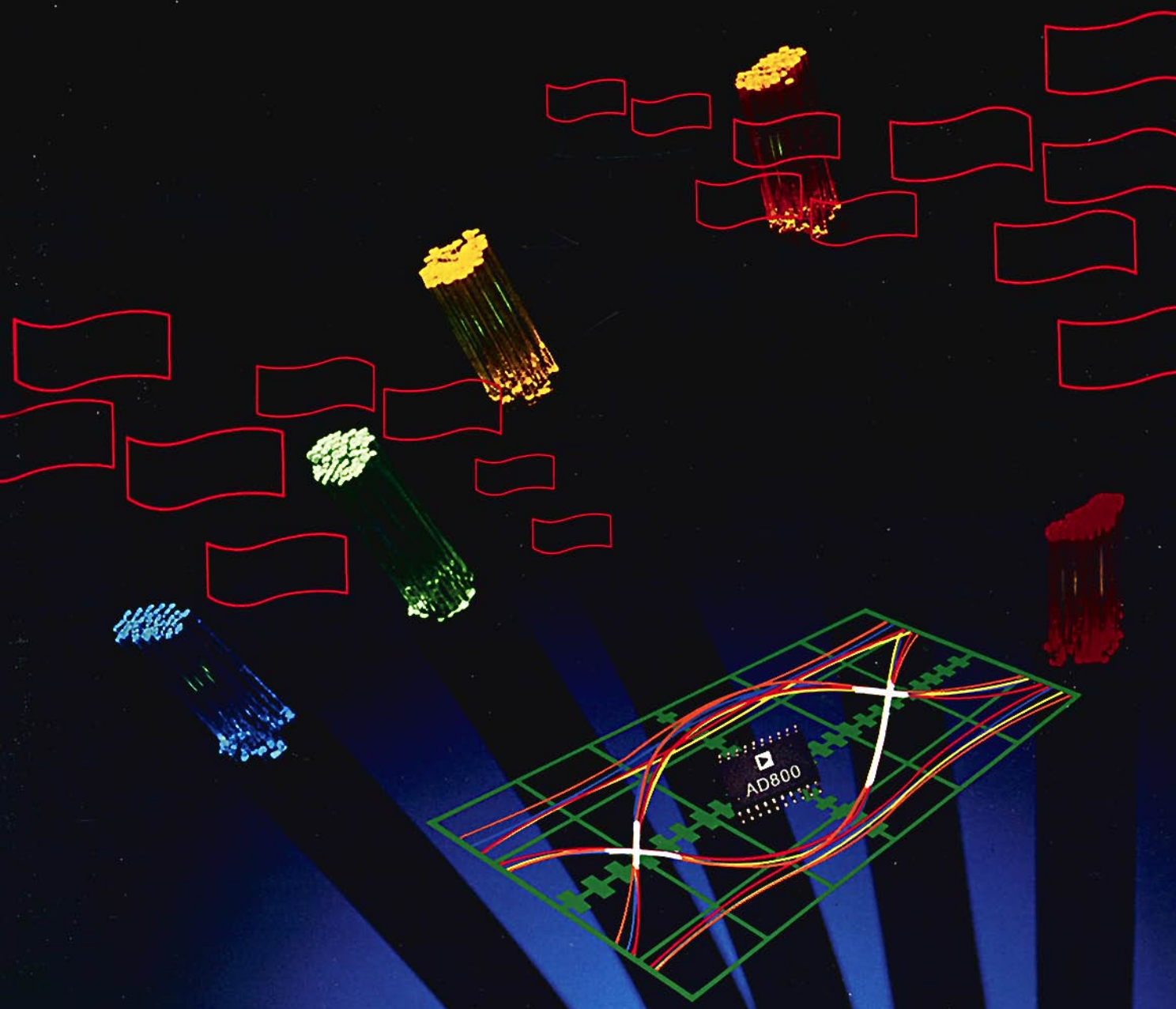
Analog Dialogue

A forum for the exchange of circuits, systems, and software for real-world signal processing



ANALOG DEVICES

Volume 27, Number 1, 1993

Editor's Notes

LOOKING BACK—AND AHEAD

As these words are being tapped out on our faithful Macintosh, we are on the threshold of January, named for two-faced Janus, the god of beginnings and of doorways—who looks simultaneously forward and backward. The simultaneity isn't so hard—if you have two faces, but still the processing of the information must be a neat trick (perhaps Janus had a dual brain). But we digress...

Twenty-five years ago (1968), our volume 2-1 featured principally op amps, and in particular, the Model 183 chopperless op amp, a 1.5" square potted discrete assembly. The *premium* L version, with a drift of 1.5 μV/°C (+10 to +60°C), was priced at $65 in small quantity. Compare that with this issue's OP-213 (page 20); the *lowest-grade* F version (−40 to +85°C), with the same drift spec—and less offset over temperature than the 183L's *initial* offset—costs less than 1/10 as much in small quantity; in the SOIC package, it is so tiny that it could easily be lost on a cluttered workbench.

Twelve-and-one-half years later (1980), our volume 14-2 showcased the 10-bit, 20-MSPS MOD-1020 sampling ADC, on a 5"×7" board, at a 100s price slightly under $2,000, and the hybrid 12-bit, 3-μs (< 0.33-MSPS) AD578. Compare them with today's *monolithic* 12-bit, 10-MSPS AD872, (and hybrid 12-bit, 25.6-MSPS AD9032) introduced on page 22.

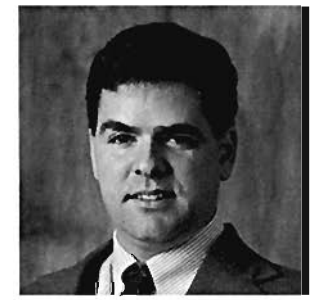
The trend to better-performing devices in smaller packages at lower prices continues, but there's more. The *kinds* of devices, their applications and markets have greatly expanded. In this issue (looking forward) you will find many topics that would have been familiar in 1980—but many more of the stories in this issue are about subjects that were little more than a gleam in our eye back then: digital signal processing, mixed-signal processing, signal computing, clock recovery for fiberoptic links, audio codecs for computers, wideband log amps, DDS components, a plethora of single-supply—including 3-volt—devices (but "give the devil his due": the popular single-supply 8-bit AD558 DACPORT® was on the *cover* of 14-2!)

RICHIE PAYNE HONORED BY IEEE

We are pleased to note that Dr. Richard Payne, of ADI's Transportation and Industrial Products Division, an IEEE Fellow, has received the 1992 IEEE Electron Devices Society's J.J.Ebers Award for "engineering achievements in process architecture and device design for twin-tub CMOS integrated-circuit technology, contributions to bipolar technology, and advancement of these technologies in commercial utilization." The Award, established in 1971, annually recognizes outstanding contributions to electron devices. Earlier recipients included John L. Moll, Andrew S. Grove, and James M. Early.

Dan Sheingold

THE AUTHORS



Fred Baechtold (page 3) is Product Marketing Specialist for the Analog Processing Group. His responsibilities include product management and product definition for very high-speed communications ICs. He received a BSEE from Northeastern University in 1981 and came to Analog Devices from Alcatel. Fred enjoys doing puzzles.

David Fair (page 7) is a Marketing Manager for the Sound Processing Group at our Wilmington site. A member of the IEEE, he holds a PhD in Philosophy of Science from Princeton University, and a BA in Physics from Pomona College. He previously worked for the Strategic Planning Institute at the University of Vermont. He enjoys listening to music, bicycling and aerobics.

Dan Williams (page 9) is a Technical Publicity Specialist at the Norwood site. His responsibilities include press releases, press relations, and technical articles. He has worked for Analog Devices for over 10 years, starting as a Product Engineering Technician on monolithic V/Fs, then working with a variety of hybrids. His interests include concert sound reinforcement, motorcycle observed trials, guitars, R & R photography and "my Beta Zero".

Mike Curtin (page 12) is a Senior Applications Engineer at our Limerick, Ireland facility, providing applications support for high-resolution D/A and A/D converters. The author of several technical articles, he holds a BSc from the University of Limerick. Mike enjoys listening to music and playing squash.

(More authors on page 30)

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Analog Dialogue

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106

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Fast, Accurate Timing Recovery for Fiberoptic Links

AD802 IC extracts timing, regenerates data at 155 Mbps with superior performance

by Fred Baechtold

The AD802-155* is the fastest of a family of IC frequency- and phase-control products for high-speed (multi-megabit-per-second) telecommunications and data-communication applications. Providing clock-recovery and data-retiming functions for data rates of 155.52-megabits-per-second (Mbps), the device is accompanied by family members with other selected data rates using the same basic design. A second-order phase-locked loop (PLL) designed to operate on ECL-level, non-return-to-zero (NRZ) serial data, it can acquire lock on random data without the aid of a preamble input data sequence.

The on-chip VCO center frequency is laser-trimmed; this guarantees loop capture and tracking ranges on input data clocked at 155.52 MHz ± 3000 ppm over operating conditions without relying on external components for VCO center-frequency setting. Just one external component is required—a capacitor to set loop damping, which determines jitter peaking.

The primary application for the AD802-155 is in SONET (Synchronous Optical NETwork) or SDH (Synchronous Digital Hierarchy)-based fiber optic receiver circuits (see the sidebar: SONET and SDH). These networking standards allow telephone operating companies to improve the cost-effectiveness of providing existing and new services. 155.52 Mbps is the lowest data rate common to SONET (North America) and SDH (Europe and Japan).

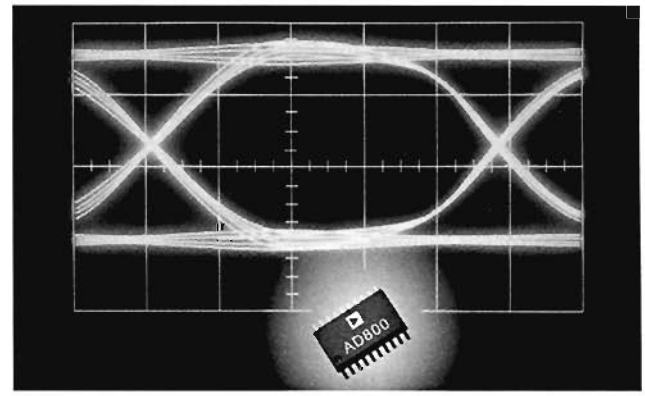
Two similar devices are available for lower speeds. The AD800-45 is for 44.736-Mbps DS-3 (T3) service, and the AD800-52 is for 51.84-Mbps OC-1 service (the lowest defined SONET rate).*

APPLICATION

In a fiberoptic communications link, the received light signal is detected (converted to current) and amplified (Figure 1). In order to deal with it as a serial binary digital signal, the clock signal must be regenerated and the properly timed binary data recovered. Thus the data-recovery circuit must first generate a clock signal to sample the reconstructed input at appropriate time instances; this sampling signal is derived from the input data stream itself. The circuit retimes data by sampling its input with the recovered clock and provides both the recovered clock and the sampled signal as outputs. At speeds >100 Mbps, accurate performance is difficult to achieve reliably.

Figure 1. Serial fiberoptic link.

*For technical data, use the reply card. Circle 3



The timing problem in a serial communications link is very different from the problem of maintaining proper timing in a processor system with parallel paths for data, along with a clock path. In those systems, data signals are just that—data. The clock needed at each point in the system is distributed along an independent, parallel path. Problems due to propagation delay can be anticipated in the design, while the relative timing between data lines and associated clock line is fairly stable (assuming the designer has been careful in layout).

In contrast, in a *synchronous* serial link, the single received signal must convey both data and clock information. The clock information is encoded in the spectrum of the data bits and can be recovered from these bits. If channel effects produce any deviations or changes from the nominal transmit clock at the receiver, they will be seen in the spectrum of the received bits as well. If the recovered clock follows those changes, the recovered data bits will retain the correct phasing.

IN THIS ISSUE

Volume 27, Number 1, 1993, 32 Pages

An *asynchronous* serial link (such as RS-232) does not derive a clock from the received data to determine the timing of the received bits; it uses a fixed independently generated local clock. But timing differences between the locally generated clock and the actual received bits will cause an unacceptable error rate beyond a 100 kbps to 1 Mbps range. Thus very high throughput rates in a practical serial link subject to timing distortions can be realized only with synchronous systems.

Channel performance is measured by applying a pseudo-random input bit sequence (mimicking real data as closely as possible) at the transmitting end and measuring the bit error rate (BER) of the retimed data at the output of the clock-recovery circuit. BER is defined as the number of bit errors measured divided by the number of bits transmitted. Fiberoptic systems in use today (in carrier networks) have BERs of less than 1×10^{-9}.

Two facts are known about the transmitted signal that will help in recovery. First, the transmit clock has a precisely known nominal frequency and accuracy tolerance, typically within 20 ppm. Second, the original binary information is generally fed through an encoder at the transmitting end; this ensures that a long block of NRZ "1"s or "0"s gets interrupted periodically by data transitions for transmission. So the circuit "knows" the range of clock frequencies that it must acquire and hold lock to (capture and tracking range) —and that it must maintain output integrity up to some specified number of transitionless bit periods.

Although the original digital pulses sent out on the optical fiber are rectangular, by the time they reach the far end they are distorted due to fiber attenuation, scattering, dispersion, and other factors. The received light signal is transformed into a current signal by a photodiode, then converted to voltage and preamplified. The resulting signal is further amplified and clipped by a buffer-and-limiter section. Though the resulting signal looks like an ideal binary pulse at first glance, errors in zero-crossing caused by the factors mentioned above cause errors in timing recovery and bit regeneration.

The parameter that principally affects the performance of a clock recovery circuit is *timing jitter*, the short-term, noise-induced variations-from-ideal of a digital signal's transitions or optimum sampling instants. "Short term" implies phase oscillations of frequency greater than or equal to 10 Hz [1].

Some or all of the input signal's jitter appears on the recovered clock, depending on the frequency of the jitter and the type of circuit used for clock recovery. In addition, the clock-recovery circuit itself adds jitter to the signal as it tries to sample the signal. This added jitter needs to be kept to a minimum, since it contributes to the probability of making a bit error. The clock-recovery circuit should ideally sample (retime) incoming data at the bit window centers, to minimize the error effect that clock jitter can have on retiming a bit. Any *static phase error* (the steady-state error between the actual sampling instant and the ideal sampling instant —at the bit window center) increases the opportunity for bit error (Figure 2).

Analysis of channel signal integrity requires special techniques at data rates greater than 100 Mbps. In addition to histogram analysis of amplitude and crossover-timing distributions, signal analysis experts have developed "eye-diagram" testing, a qualitative visual approach to high-bit-rate signal analysis at various points in the system [Ref. 2]. This involves capturing and superimposing, on an oscilloscope, multiple data pulses synchronized with the recovered clock, producing an eye-shaped pattern (Figure 3).

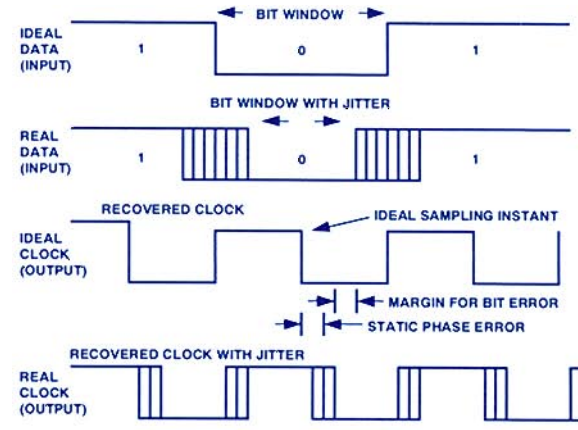


Figure 2. Clock jitter and static phase error cause regeneration of bits with errors; more margin means fewer bit errors.

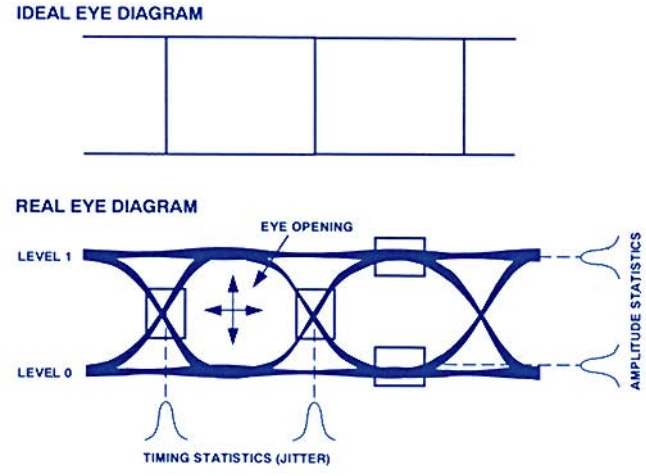


Figure 3. "Eye" diagrams (ideal and real) provide information about noise and jitter in the signal.

A data signal with a large eye opening is less likely to have bit errors than one with a smaller opening. Performance is tested to industry standards by comparing a signal's eye diagram to a template bounded by minimum and maximum acceptable values. The eye diagram is a valuable tool for judging the channel, both statically and dynamically. The width and density of the pattern around the zero crossings shows the timing jitter, while the opening of the eye shows noise and attenuation. As the channel characteristics change, or the receiver is adjusted (e.g., by parameter changes in the front-end circuitry), the eye pattern responds immediately.

ARCHITECTURE OF THE AD802

The AD802 (Figure 4) features a frequency loop and a phase loop; they are inherently coordinated, since frequency is the rate-of-change of phase. The frequency loop performs a quick but coarse acquisition, necessary when lock is being initially established. The center frequency of the AD802 VCO is factory-trimmed to guarantee loop capture and tracking ranges over the operating temperature range. Trimming eliminates the usual need for a crystal or other external resonant network to aid initial frequency acquisition, experienced with other PLL chip designs.

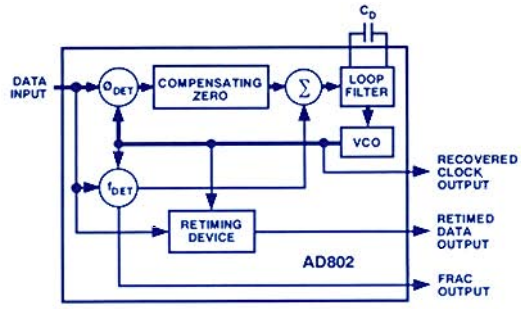


Figure 4. AD802 block diagram.

The phase-acquisition loop takes over automatically after frequency lock, tweaking the VCO to keep the output phase tracking the input phase. The frequency detector is always active, but with zero effect after frequency lock (except to detect and correct loss of lock). No external mode control signal is needed to instruct the device to go from frequency to phase lock operation. Other PLL ICs require an external mode-control signal to initiate acquisition in steps—first frequency, then phase; they also require a monitor to detect loss of lock and initiate a recovery sequence any time lock is lost. [see Sidebar: Recovery/Regeneration Techniques]

The user sets the loop damping of the AD802 with a single external capacitor, whose value determines the jitter peaking. A damping factor of 5 corresponds to jitter peaking of 0.08 dB, a damping factor of 10 to jitter peaking of 0.02 dB.

The AD802 can lock onto incoming data that is random, without requiring some specific preamble data pattern for frequency/phase lock. Requiring a preamble is acceptable for PLLs used in local-area networks, since data has a burst-like quality and handshaking is used to establish node-to-node connections. In such networks, minimizing the length of the preamble is important but not a priority to increase real data throughput. But telecommunication systems are typically point-to-point, with a data flow that is continuous, not burst-like.

Using a patented phase detector, the AD802 virtually eliminates jitter caused by variations in the density of data transitions (*pattern jitter*). For a pseudorandom code pattern of 2^7-1 bits, the jitter created by the AD802 is just 1°, the same as for a longer, less-repetitive $2^{23}-1$-bit random pattern.

The AD802's bandwidth is factory-set by mask option to 0.08% of the data rate (from a mask-programmable range of 0.01% to 1.0%). We chose the 0.08% figure to be compatible with the jitter-tolerance and jitter-transfer templates for an SDH Type A Regenerator (CCITT Recommendation G.958). An AD802 with a very low loop bandwidth would be effective in filtering a jittery timing signal, but at the cost of decreased wideband jitter tolerance.

Jitter tolerance measures the PLL's ability to track a jittery input data signal. As jitter on the input data increases, measured in *unit intervals* (or bit periods), the PLL starts to make errors. Figure 5 shows the jitter tolerance (A) and the standard tolerance "mask", or limit (B), plotted as unit intervals vs. jitter frequency.

The frequency and phase acquisition time for the AD802, roughly 1 million (M) bit-periods, is appreciably longer than the 100-bit-period acquisition time for SAW filter MCMs. However, at 155 Mbps, 1-Mbit periods (< 1/100 second) are negligible, since the system in normal operation should maintain lock continuously over 20 years. (If lock is lost in a telecommunications fiberoptic system, it is probably because a backhoe has dug up the fiber!)

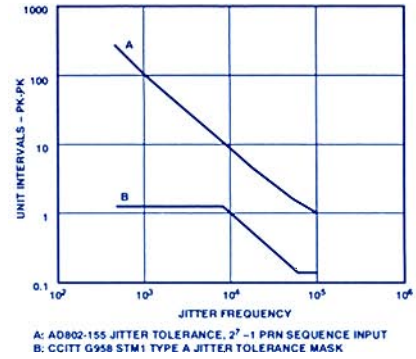


Figure 5. Jitter tolerance in unit intervals as a function of jitter frequency.

The AD802 maintains lock through a transitionless (all 1s or 0s) data run of up to 240 bits; competitive units can function only with transitionless runs up to 60 bits. Total loop jitter is 20° peak-to-peak, and jitter bandwidth is 130 kHz. Operating from a single −5.2-V supply, it typically dissipates 750 mW and is compactly housed in a 20-pin SOIC. Price of the AD802-155 is $56 in 1000s; the AD800-52 and AD800-45 are $30 in 1000s.

The AD802-155 was designed by a team headed by Larry DeVito at Analog Devices, Wilmington, MA.

(continued on page 6)

SONET and SDH

Fiberoptic systems were originally installed as point-to-point links between long-distance major system nodes (such as metropolitan service areas or industrial parks). Now SONET and SDH are designed to bring fiber capacity to local users.

Defined in 1985, the SONET/SDH standard, set by representatives of North American, European, and Japanese interexchange and local-exchange telephone companies, specifies synchronous multiplexing techniques and standard fiberoptic data rates from 51.84 Mbps to 2.4 Gbps, in 51.84-Mbps increments. Fiberoptic terminal equipment, using synchronous multiplexing techniques can subdivide the number of samples and provide smaller users with service data rates of 1.544 Mbps or 2.048 Mbps (or multiples) directly to or from the fiber data rate, without the need for intermediate multiplexers.

Although fiber has major advantages in cost and reliability over copper cable for high-capacity, long-distance communications, fiber has yet to penetrate the segment of the telephone-company network that extends from the switching office to the subscriber, or "local loop." Only about 10% of this segment has fiber systems now. SONET/SDH helps eliminate impediments to fiber's use in the local loop by establishing a non-proprietary standard. This is in welcome contrast to the difficulties and costs of using different vendors' proprietary fiberoptic terminals, as well as the costs of intermediate multiplexers needed to multiplex/demultiplex services to and from the fiber.

SONET/SDH define standard data rates, data formats, optical parameters, signal scrambling, control and maintenance procedures, and performance monitoring. This means, for example, that a telephone company can install a SONET/SDH 155.52-Mbps system using terminals from two different vendors providing SONET/SDH-compliant 155.52-Mbps terminals. It can also provide users with sub-channels in multiples of 1.544 and 2.048 Mbps.

References *(Not available from Analog Devices Literature Center)*

1. *Transport Systems Generic Requirements (TSGR): Common Requirements*, A module of TSGR, TR-TSY-000440, Issue 3, Bell Communications Research, December 1989.
2. V. Prasannan and Kevin Smith, "New Communications Standards Require Specialized Test," *Electronic Design*, December 5, 1991.
3. Jim Lane, Telco Systems, "Asynchronous Transfer Mode: Bandwidth for the Future," 1992.

RECOVERY/REGENERATION TECHNIQUES

Two established techniques for clock recovery and data retiming of 155-Mbps data are resonant circuits and phase-locked loops.

The predominant circuit in use for >100-Mbps clock recovery integrates a surface-acoustic-wave (SAW) filter with other electronics in a multi-chip module (MCM). A SAW filter comprises an acoustic resonator (e.g., lithium niobate) with electrical input and output transducers. Each time the input data makes a transition, a pulse excites the high-Q SAW resonant filter, which is tuned to the clock frequency, providing a damped sine wave output. The sine wave edges get "squared-up" by the limiting amplifier to create the recovered clock signal. A delay element makes up for the phase difference between the input data and the recovered clock.

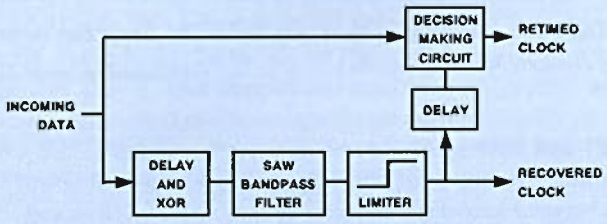


Figure SB-1 Resonant filter block diagram.

Since SAW filters cannot be manufactured with exactly equal phase delays, each device's delay element needs to be trimmed to match its SAW filter to minimize the sampling clock's static phase error. SAW filters have excellent phase stability over frequency, time and temperature—to avoid large static phase errors.

Since the SAW filter MCM architecture is open loop, a loss of input data (no transitions for a long period of time) means a loss of output clock. However, the devices typically capture lock on incoming data within 100 bit-periods. The SAW filter starts oscillating quickly, and the limiting amplifier (fast comparator) can provide full-scale signals from low-amplitude oscillations.

Resonant-filter-based clock-recovery-and-data-retiming circuits require a significant tradeoff between static phase error and jitter attenuation. The center-frequency inaccuracy of the resonant filter contributes linearly to the circuit's static phase error, and the filter's Q magnifies any static phase error caused by center-frequency offset. To minimize this, a designer needs to limit the resonant circuit's Q. However, limiting the Q limits the circuit's ability to attenuate high-frequency input jitter. Thus the no-win tradeoff is between poor jitter attenuation due to low Q and greater static phase error due to off-center-frequency error.

The *phase-locked-loop* (PLL) technique for clock recovery makes use of a negative-feedback control loop to generate a new waveshape with frequency and phase that follow the input frequency and phase. The phase detector continuously compares the phase of the recovered clock—generated by a voltage-controlled oscillator (VCO)—with the incoming data. The loop amplifier and filter process this error signal to produce a voltage that drives the VCO to a frequency and phase that closely track the incoming data phase. The VCO's output is the recovered clock signal, and it is used to sample the data.

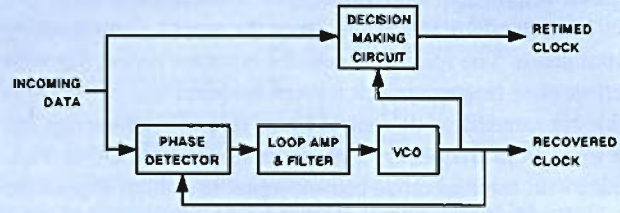


Figure SB-2. PLL block diagram.

Where the center frequency is known to reasonable accuracy, as in the cases described here, typical PLL circuits require a stable (externally derived) frequency-acquisition aid, like a voltage-controllable crystal oscillator, or a crystal, to set the VCO to an accurate enough center frequency (±50 ppm from nominal) to permit phase locking.

Traditional second-order PLL circuits require a zero in the transfer function's forward path for loop compensation. The presence of this zero translates to "jitter peaking" in the closed-loop transfer function. This means jitter gain is greater than 0 dB (unity) for signal jitter components at frequencies within the circuit's jitter bandwidth. The effect is usually minimized by overdamping the loop—but at the cost of longer acquisition time. Unlike the SAW-filter MCM, the PLL circuit always provides a nominal clock output, even when input data levels don't change.

The table summarizes the physical and economic tradeoffs of the SAW-filter MCM and traditional PLL circuit design for use in high-volume applications in SONET/SDH systems. The outlook for PLLs is greatly improved by the architecture of the AD802.

Tradeoffs: SAW filter and Conventional PLL

SAW filters:

- High production cost of MCMs:
  Need to match circuit elements to each other
  Multiple test steps.
- Poor high-frequency jitter attenuation:
  High frequency jitter accumulation in system with multiple SAW-filter MCM-based regenerators
- Loss of input data means loss of clock.

PLLs (prior to the monolithic AD802):

- High production cost:
  Circuit needs VCXO or precision network for frequency acquisition aid
- Sensitivity to input jitter:
  VCXO tuning range limits circuit ability to lock onto jittery input.

SoundPort® Codecs: Complete Audio I/O Subsystem ICs for Workstations and PCs

AD1848 and AD1849 feature stereo in/out, microphone input, amplifiers, and parallel bus or serial link interface to processor

by David Fair

The AD1848* and AD1849* 16-bit SoundPort® Stereo Codecs (coder/decoder) bring "audio system on a chip" integration to computer applications for multimedia sound and business audio. Operating from a single +5-V supply, they allow sophisticated digital audio functions to be incorporated on PC or workstation motherboards or add-in boards easily and at low cost.

Both codecs include stereo sigma-delta analog-to-digital (a/d) and digital-to-analog (d/a) converters, with their 1-bit, high-sampling-rate analog interface (*Analog Dialogue* 26-1, p. 8). They achieve a dynamic range of 80 dB with total harmonic distortion plus noise of −74 dB over the 0-to-20-kHz audio band. They are fabricated in a digital CMOS process enhanced with a second layer of polysilicon to facilitate high-performance capacitor formation.

These codecs offer far more than just two pairs of integrated converters. On-chip oscillators provide for software selection of all the key multimedia sample rates from 5,500 samples/second to 48 ksps, via software selection of one of two external crystals and the appropriate division ratio; an external clock may also be supplied. Signal filters are provided on-chip to simplify design and reduce expense and space requirements. The sigma-delta a/d converters incorporate their own digital decimation filters with maximum ±0.1-dB passband ripple. The d/a converters are preceded by an integral interpolation filter in the digital domain and followed by switched-capacitor and continuous-time analog filters to remove Nyquist images. No external references are required; they are included on the SoundPort codec chips.

In addition, both devices allow independent control of left- and right-channel input gain in 1.5-dB steps, from 0 to +22.5 dB. Microphone inputs have access to an additional +20-dB gain block. Left- and right-channel outputs can be attenuated from 0 dB to −94.5 dB, in 1.5-dB steps, or muted (shut off entirely). Both codecs support mixing of the a/d converter's output with the d/a converter's input for audio overlay ("karaoke" operation) under software control. The devices support pulse-code-modulated (PCM) 16-bit linear, 8-bit companded μ-law, and 8-bit companded A-law data formats.

The AD1848 and AD1849 SoundPort codecs are basically similar; they differ principally in their digital interface. The AD1848 (Figure 1) has a byte-wide parallel data/control port that supports a buffered direct connection to the Industry Standard Architecture (ISA) or " PC-AT" bus. This AD1848 format was specified in a joint agreement between Analog Devices, Inc., Compaq Computer Corp., and Microsoft. Its objective was to provide the lowest cost and simplest implementation of digital audio capabilities in an ISA-bus system.

*Use the reply card for AD1848 technical data. For AD1849, phone Applications at (617) 937-1428. For AD1848 circle 4

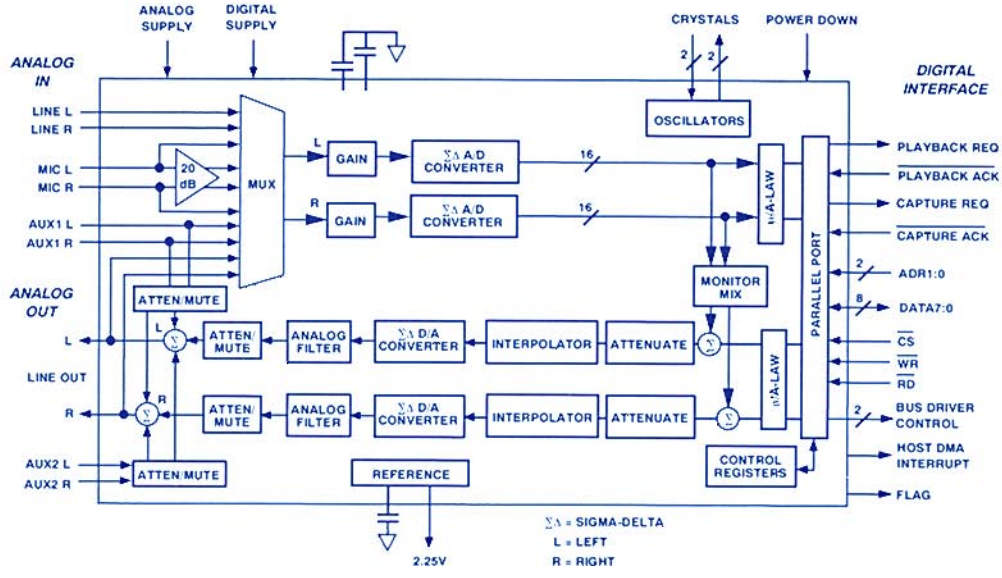


Figure 1. Parallel AD1848 block diagram.

Compaq uses the AD1848 in the newly announced DESKPRO® computers, and Microsoft uses it in their Windows Sound System® board. Since the precision AD1848 audio system cannot be expected to drive the capacitance of the ISA bus directly, the interface uses an external '245-type digital bus transceiver for current buffering—but under control of the AD1848; it provides the Enable and Direction signals for the transceiver (Figure 2).

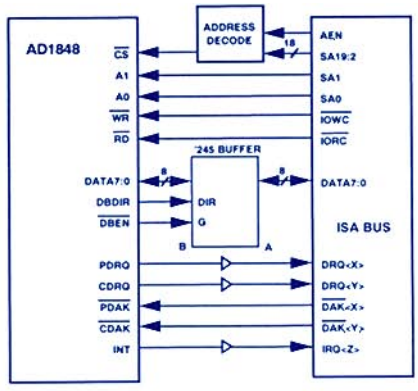


Figure 2. AD1848-to-PC bus interface.

In contrast, the AD1849 (Figure 3) uses a *serial* interface for data and control information. This SoundPort was developed to meet the needs of Sun Microsystems Corporation's SPARCstation 10 series of UNIX workstations. Sun's original requirement for the serial interface was that it connect with the ISDN bus employed in these new SPARCstations using minimal translation logic. Fortunately, the serial interface is general enough to allow direct or very simple connection to the serial ports of digital signal processors, including popular members of the ADSP-2100 family—as well as DSPs from other vendors.

The direct connection to DSPs makes it possible to design very cost-effective digital audio "signal-computing" solutions (*Analog Dialogue* 26-2). The DSP can implement a wide range of compression/decompression and audio effects algorithms (such as filtering or equalization) using programs that can be either ROM-resident or downloaded from disk into local RAM.

Additional features of—and differences between—the AD1848 and AD1849 make available solutions for a variety of user needs. For example, the **AD1848** parallel-port codec supports both programmed I/O (PIO) and direct memory access (DMA) transfers. In PIO, control information is transferred using the Read and Write strobes. Five registers are directly addressed via the two address pins of the IC. Two of these, used for address and data, indirectly access 16 additional byte-wide control registers, minimizing the number of PLCC package pins (68). Either one or two channels of DMA are supported via the Request and Acknowledge controls. A loadable, 16-bit DMA down-counter generates an external/internal interrupt on underflow.

For multimedia PC (MPC) compatibility, the AD1848 also has two stereo pairs of auxiliary line-level *analog* inputs. Both channels can be independently mixed with the stereo DAC output in the analog domain. As the block diagram shows, this post-mixed analog signal is itself available as an input to the stereo a/d converters. The AD1848 also supports the MPC standard's 8-bit unsigned data format at input and output.

The **AD1849** serial-port codec has its own share of unique features. It will accept one of three clock sources: an external crystal, an external clock, or the serial port's bit clock. The serial bus can support up to four devices via time-division multiplexing (TDM). It also has chaining inputs and outputs for sequential word synchronization when one, two, or four devices are "daisy-chained" on a single serial bus. Though more limited than the AD1848 with respect to analog inputs, the AD1849 offers an additional line-level stereo output driven from the stereo d/a converters, and an additional output for a monophonic speaker. The AD1849 is packaged in a 48-lead PLCC.

These two SoundPort codecs provide complete solutions for computer digital-audio applications requiring either parallel or serial interfacing. Though differing in detail, their capabilities are comparable overall. In 1000s, the parallel-port AD1848 is priced at $33 and the serial port AD1849 at $30.

These ICs were designed by a team led by Tom Guy, in Wilmington MA, and Jim Wilson, in Norwood MA.

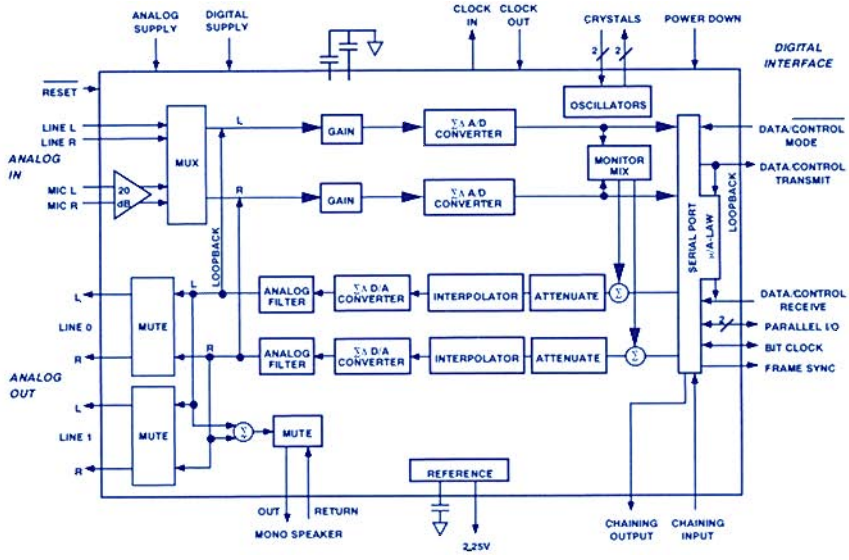


Figure 3. Serial AD1849 block diagram.

ADI's Smallest, Lowest-Cost Signal-Conditioning Modules for Process Control

The 1500-V isolated 7B series handles voltage, current, RTD, and thermocouple inputs, plus process-I and V outputs

by Dan Williams

We've all seen it on the late movie. The scientist, working alone in his laboratory, surrounded by Bunsen burners and beakers of unknown fluids, holds one beaker to the light. With a single swift motion he drinks the contents, usually with disastrous results—prompting us to ask, was the good doctor really that bad a chemist or just a victim of inadequate process control?

Today, automated factories producing everything from gasoline to breakfast cereals to movie film use sensors and signal conditioning electronics for process-monitoring and control—a technology that makes the difference between a smooth-running, profitable production line and a costly B-movie monster of safety and quality problems.

INTRODUCING THE 7B SERIES

The 7B series* of single-point signal conditioning modules from Analog Devices have evolved from the highly successful 5B series (*Analog Dialogue* 20-2, 1986). Designed to meet the demands of the process control industry, the 7Bs are the smallest and lowest-cost complete, isolated, analog input to analog output signal-conditioning modules available.

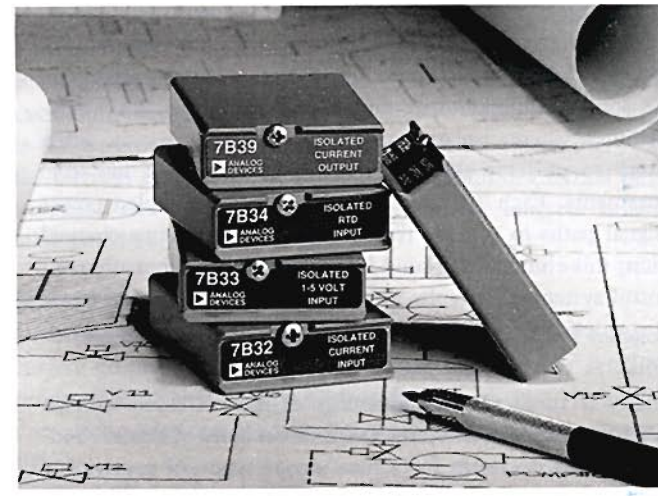
When combined with a PC-compatible data-acquisition board, such as Analog Devices RTI-834, and commercially available software packages, such as LABTECH™, a 7B based system becomes a powerful data-acquisition-and-control tool.

Input modules accept signals from thermocouples, resistance temperature-detectors (RTDs), millivolt- and volt-level sources, as well as process-current signals, and are chosen to provide +1 to +5-volt or 0 to +10-volt output. *Output modules* accept high-level analog signals and are chosen to provide either 4 to 20 mA, 0 to 20 mA, or ±10-volt process signals.

All 7B modules are factory-calibrated to guarantee maximum nonlinearity of ±0.02% and accuracy to within +0.1% of the span. Powered from a nominal +24-V dc (a customary supply voltage in control systems), the 7B series can operate with dc supply voltages ranging from +14 volts to +35 volts. The transformer-isolated 7B series use amplitude modulation to handle signals at frequencies all the way down to dc.

The block diagram of Figure 1 illustrates the basic configuration of a 7B module. The input section contains input-protection circuitry and filters, and—in the case of the thermocouple-input 7B37—cold-junction-compensation circuitry; a low-drift amplifier provides gain, an isolated dc power supply powers the active components on the input side of the module, and a modulator translates the input signal for passage across the transformer. The output section contains a demodulator for recovery of the input signal, a two-pole low-pass filter, a buffer amplifier and a power oscillator. The low-pass filter reduces carrier noise, and the buffer amplifier provides a low-impedance signal at the output terminal. Isolated dc power for the input-side electronics is derived from the power oscillator.

*Use the reply card for technical data. Circle 5



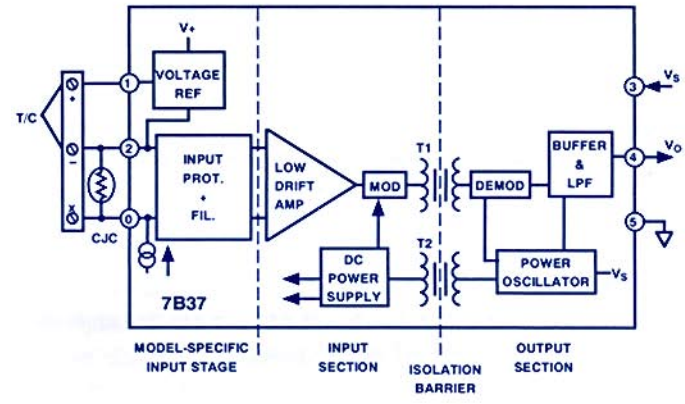


Figure 1. Functional block diagram of the 7B37 isolated thermocouple signal conditioner.

WHY MODULES?

Once the sole domain of large-integrated-system providers, industrial automation has undergone a revolution in the past few years due to the advent of powerful and inexpensive computers. They have provided easier-to-use tools that system users can employ to design, modify, and custom-tailor process monitoring-and-control systems to fit their actual needs.

Modular signal conditioners have proved to be the ideal link between these machines and the process sensors and actuators; they offer unprecedented flexibility and a cost-effective method of protecting sensitive electronics from the harsh realities of the factory floor. Process control often involves the connection of a central controller to machinery separated by hundreds or thousands of feet of cabling, possibly connected to different power systems and usually operating in electrically noisy environments. Transients, ground loops and potentially dangerous common-mode voltages, destructive to computer and measurement equipment, are common threats.

One of the most important functions of an isolated signal conditioner is to protect the control system, its operators, and the vital process data from these hazards. Such isolation is also useful even in the somewhat less-hostile environments of laboratory data-acquisition, where isolation of individual sensors is often necessary to preserve the resolution and accuracy of low-level measurements. Each 7B module has transformer-coupled power and signal paths to provide true galvanic 1500-volt-rms channel isolation; this eliminates ground loops, protects the measurement & control system from faults that may occur in the field wiring, and provides high common-mode rejection to maintain signal integrity.

Flexibility is another major advantage of module-based systems over integrated sensor interfaces and user-designed systems. Modifying a 7B-based system for a new sensor type—or repairing a defective channel—is as simple as changing a module. All that is required is a small Phillips screwdriver. In a laboratory where a test system may test the controller of a washing machine one day and an air-conditioner the next, the ability to quickly and easily reconfigure system I/O is critical. A significant feature of the 7B series is that modules can be replaced with power on. This often eliminates the need to power down an entire system to replace a single measurement point—a vitally important feature in applications where shutting down an entire process to replace a backup sensor or a relatively unimportant measurement point would be extremely costly.

All 7B modules are identical in size (1.66" × 2.11" × 0.600", 42 mm × 54 mm × 14 mm) and pin configuration, allowing users to configure the system to meet their needs. Unlike most other signal conditioning modules, the 7B's simple six-pin interface and small footprint allow installation on 0.625" centers—making available much higher channel density than other modules. However, conductors must be spaced so as to maintain the specified degree of isolation and conform to code requirements if the user elects to design a specialized backplane.

RELIABILITY

Specified for operation over the −40 to +85°C temperature range, the 7B module is potted in a sturdy plastic case to seal out contaminants and permit use in high-humidity (non-condensing) environments There are no external adjustment potentiometers; this minimizes the chance of mechanical or human errors being introduced into the system. The modules are fully protected from field-wiring faults to 120-V rms line voltage; furthermore, the isolation prevents such faults from propagating through the module and backplane into the main system. Designed to be electrically robust, all 7B-series modules meet the IEC 255-4 Class II and IEEE STD-472 transient standards as well as IEC 801-2, Level 2 standard for ESD.

INPUT MODULES

Temperature

The great majority of sensors for process control provide temperature measurements. For applications ranging from what temperature to cook the hops at in brewing beer to the correct plastic temperature for an injection molding machine to the correct annealing temperature for thermocouple wire, a wide variety of thermocouples, RTDs, and silicon temperature transducers must be accommodated. Two of the 7B modules are designed specifically to interface with the most common temperature sensors —thermocouples and RTDs.

The **7B37** isolated thermocouple input accepts input from J, K, T, E, R, S, and B type thermocouples and provides an amplified +1 to +5-volt or 0 to +10-volt output. The 7B37 provides upscale open-thermocouple detection and is designed to accept cold-junction compensation (CJC) from a thermistor mounted on the backplane adjacent to the field-wiring terminals. Cold-junction compensation provides an ambient temperature reference, correcting for non-zero temperature at the reference junction between the thermocouple wires and the backplane terminals. Standard ranges are available for each thermocouple type. The 7B37 uses three input pins, including the CJC input. All three inputs are protected against 120-volt faults in the field wiring.

The **7B34** accepts input from 100-Ω platinum RTDs (α = 0.00385) and provides an output voltage (+1 to +5-volt and 0 to +10-volt ranges) that is linear with temperature. The module has a noise-reduction filter with a 3-Hz bandwidth; three-wire lead compensation allows the use of 2-, 3-, or 4 wire RTDs. To minimize drift due to heating of the platinum RTD, the module's sensor excitation current is kept to 0.25 mA. A current source identical to the excitation current source is connected to the third lead of the RTD to compensate for the resistance of long leads.

Process Voltage and Current

In addition to dedicated thermocouple and RTD conditioners, five 7B series modules have been designed to interface with the wide variety of voltages and currents encountered in process control.

Table 1. Available Input and Output Modules

Input Module	Input Type/Ranges	Voltage Output
7B21	Voltage: ±10 V	±10 V
7B30	Voltage: 0 to +10 mV, 0 to +100 mV, ±10 mV, 0 to 1 V, ±100 mV, 1 V to 5 V, ±1 V Current, with external 250-Ω sense resistor: 4 to 20 mA, 0 to 20 mA	1 to +5 V, 0 to +10 V
7B31	Voltage: 0 to 5 V, 0 to 10 V, ±5 V, ±10 V	1 to +5 V, 0 to +10 V
7B32	Current: 4 to 20 mA, 0 to 20 mA	1 to +5 V, 0 to +10 V
7B33	Current: 0 to 20 mA Voltage: 1 to 5 V, 0 to 5 V	1 to +5 V, 0 to +10 V
7B34	Platinum RTD 2 or 3 wire α=0.00385, 100 Ω −100°C to +100°C, 0°C to +100°C, 0°C to +200°C, 0°C to +600°C	1 to +5 V, 0 to +10 V
7B35	2-wire transmitter current: 4 to 20 mA, provides loop power	1 to +5 V, 2 to +10 V
7B37	Thermocouple Types J, K, T, E, R, S, B	1 to +5 V, 0 to +10 V
Output Module	**Output Type/Span**	**Voltage Input**
7B39	Current: 4 to 20 mA, 0 to 20 mA	1 to 5 V, 0 to 10 V
7B22	±10 V	±10 V

The **7B21** bipolar voltage-input module has a full scale input range of ±10 volts. With its unity gain, the 7B21 is intended to provide isolation for high-level signals that simply require a differential measurement to remove common-mode voltage. The **7B33**, similar to the 7B21, isolates a +1 to +5-volt input signal and provides a buffered +1 to +5-volt output. The **7B30** and **7B31** accept dc input voltages and provide a factory-configured +1 to +5-volt or 0 to +10-volt output signal. The 7B30 is available with standard input ranges from ±10 mV to ±1 volt, while the 7B31's choice of input spans ranges from ±1 volt to ±10 volts.

For 4-to-20-mA process currents, the **7B32** incorporates a protected, factory-calibrated current-sensing input resistor. Process currents can be connected directly to the module without compromising system integrity. The 7B32 features a +1 to +5-volt output range and has a 100-Hz bandwidth.

Two-Wire Transmitters

The **7B35** 4-20 mA current input module (Figure 2) is unique: besides measuring and conditioning process signals from current transmitters, it provides the +24-volt (nominal) isolated loop power necessary for excitation of its associated two-wire transmitter, thus eliminating an external power supply.

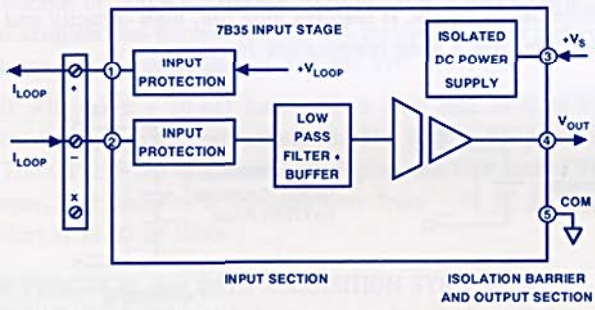


Figure 2. Functional block diagram and input/output connections of the 7B35 2-wire transmitter interface module.

The two-wire transmitter, a common method of protecting low-level sensor signals from the electrical interference often found in industrial applications, transmits sensor information in the form of current (typically 4-to-20 mA), over a pair of wires that are part of a series loop. Since the loop current can be measured independently of voltage, any noise voltage picked up in the connecting wires is ignored. Some two-wire transmitters are provided as separate units to interface with the sensor and are powered from loop supplies; but increasingly the transmitter is becoming an integral part of a complete sensing unit—flowmeter or temperature sensor.

Since many of these transmitters are designed to be powered from a source in the output loop, there are evident advantages to an isolated conditioner, such as the 7B35, that can provide loop excitation. Besides making it unnecessary to place a power supply in the hazardous operating environment of the transmitter— and the obvious cost saving due to the elimination of external power supplies, users of the 7B35 benefit from the inherent isolation maintained between channels.

OUTPUT MODULES

Often there is a need for the system to provide a control voltage or current to operate process control elements, such as actuators, proportional valves, electric heaters, or motors. The 7B family at present includes two modules designed to output isolated control signals.

The **7B22** is a unity-gain *voltage*-output module with a range of ±10 volts. Along with its 1500-volt isolation between the control system and the field wiring, the 7B22 also provides 100 dB of common-mode voltage rejection with a 400-Hz bandwidth. To provide process-control *current*, the **7B39** (Figure 3) accepts a +1 to +5-volt or 0 to ±10-volt signal from the system and outputs a galvanically isolated 4-to-20mA or 0-to-20 mA to the field wiring; it is capable of driving a 750-Ω load with power from a 24-volt supply.

ACCESSORIES

Backplanes

Accessories available from Analog Devices to facilitate use of the 7B series include a set of 4-, 8-, and 16-channel backplanes: the **7BP04-1**, **7BP08-1** and **7BP16-1**. These backplanes are designed for ease of use with the 7B series modules. All backplanes provide a set of three I/O screw terminals for each channel, plus a CJC thermistor for use with thermocouples. Two identical 25-pin I/O connectors, available to all channels, can be used for high-level voltage I/O, permitting redundant cabling in critical applications —or separate connections for input and output signals in applications where both types of modules are used on the same backplane. To guard against power disruptions in operation, users can connect redundant power supplies, using the diode isolated power-supply screw-terminals. A light-emitting diode (LED) indicates when power is present.

Other 7B accessories include cables, interface boards, rack-mount kits, and blank modules for users' special-purpose auxiliary circuitry. Prices of the modules, depending on function, range from $85 to $105 in 100-piece quantities.

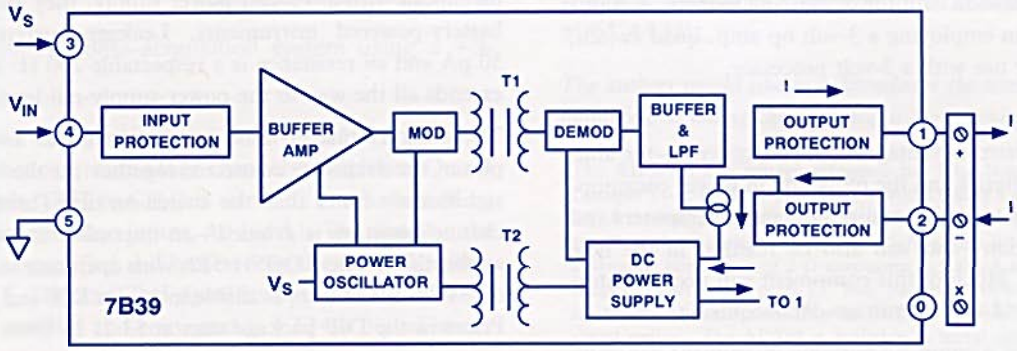


Figure 3. The 7B39 current-output module.

3-Volt-Supply 12-Bit Multi-Channel Data-Acquisition System Samples at 50 kHz

Low-voltage single-supply ADCs, op amps, switches, & references save power in battery/portable instruments and equipment

by Mike Curtin and Matt Smith

Three-volt systems and their uses

For some years, there has been a need for analog, digital, and interface ICs that operate from single supply voltages, usually +5 volts; many products are available from Analog Devices and other companies to meet this requirement. More recently, however, interest has grown in devices that can operate from a 3-volt supply for use in battery-powered systems and instruments. Because of the freedom and mobility imparted to the user, such untethered equipment is extremely attractive and will become even more so as the cost of 3-volt active devices decreases. Lower voltage means fewer batteries, lower power means longer life with increased reliability (from running cooler and with lower internal stress voltages).

Where will 3-volt systems be used? Examples include such low-power portable equipment as laptop computers, mobile radios and portable instrumentation. The recently unveiled low-voltage versions of the popular and powerful '386 and 680X0 microprocessors allow laptop computers to operate from 3-volt supplies, resulting in a significant reduction in overall power consumption. In addition, mobile radio equipment will soon have the benefit of 3-volt digital signal processors (the ADSP-2103 from Analog Devices, to be discussed in the next issue, is one of the first).

Analog Devices currently manufactures parts that meet this requirement and has an active program to increase both the scope of available parts (from op amps to digital signal processors) and the range of available specifications. The existing and forthcoming 3-volt ICs from Analog Devices will complete the picture and allow real-world signals to be acquired and processed in 3-volt-based instrumentation and signal computing systems with varying performance requirements.

In this article, we discuss some of the technical considerations of 3-volt systems and conclude with the design and performance of a data-acquisition system employing a 3-volt op amp, quad switch, and a/d converter, for use with a 3-volt processor.

Advantages

There are two interrelated advantages of 3-volt systems—the ability to operate from batteries and the reduction in power consumption. These advantages are being realized in laptop computers and portable instrumentation—and will also be realized in the new pen-based computers. Much of this equipment will need to interface to the analog world via low-voltage data-acquisition chips.

Because all elements of a complete portable instrument generally operate from a single set of batteries, it is imperative that power consumption be kept to a minimum. Thus, 3-volt devices have a distinct advantage over those using 5 volts because, in general, the power consumption of CMOS devices varies with the square of the power-supply voltage. Thus, the typical power consumption of a device operated at 3 volts will only be 36% of that consumed at 5 volts. This saving in power consumption can extend the system battery's life significantly.

Low-Voltage Standards

There are two standard "3-volt" ranges emerging for battery-powered systems. They are: 3.3 V ± 0.3 V and 3 V ± 0.3 V. The latter would be suitable because two standard 1.5-volt cells could be used to obtain the required design-center voltage. However, the former seems on its way to becoming the *de facto* standard. The '386, 680X0 and the ADSP2103 are all specified for this supply range. In addition, JEDEC has proposed this as a low-voltage standard, under the designation: JEDEC LV standard (8.1).

The Analog Devices parts mentioned in this article, specified for the 3.3 V ± 0.3 V supply range, are compatible with the proposed JEDEC LV standard.

Two ways of making a 3.3 volt supply using standard cell types are shown in Figure 1. Option A consists of a lithium (Li) cell, which generates 3.5 volts. It features long life, high capacity and good operation over a wide temperature range.

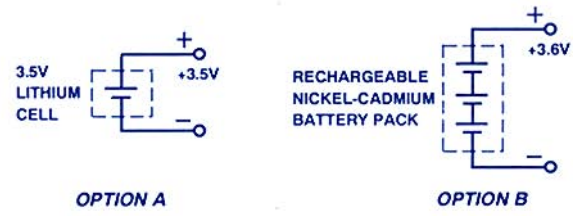


Figure 1. Typical battery power supply.

An alternative, Option B, uses 3 rechargeable nickel-cadmium (Ni-Cd) cells to generate 3.6 volts. These cells feature excellent cycle life with flat discharge characteristics, and they can sustain high discharge rates.

EXAMPLES OF DEVICES FOR +3-V OPERATION

ADG511/512 Quad Switches: The ADG511 and ADG512* are quad CMOS single-pole, single-throw (SPST) switches fully specified for +5-V and ±5-V—as well as +3-V—power supplies; they differ from one another only in the polarity of signals required to turn a switch on. With their ultra-low power dissipation—3 μW maximum with a +3-volt power supply, they are ideal for use in battery-powered instruments. Leakage currents are typically 50 pA and *on* resistance is a respectable 200 Ω. The signal range extends all the way to the power-supply-rail levels.

To configure one of these quad switches as a 4-channel multiplexer, the drains are connected together. As the switch-off time is significantly faster than the switch-on time (break-before-make), channel shorting is avoided—an important factor in multiplexer applications. The ADG511/512, with operating temperature range of −40 to +85°C, are available in 16-pin DIP and SOIC packages. Prices in the DIP package start at $3.21 in 1000s.

*Use the reply card for technical data. Circle 6

AD7883 12-bit A/D Converter: The AD7883* is a high-speed, low-power, 12-bit sampling A/D converter specified for 3-volt operation. It is characterized for a 50-kHz throughput rate and is specified for both ac parameters—such as harmonic distortion and SNR—and dc parameters, such as accuracy and linearity. It is suitable for a broad range of applications, from industrial process control to digital signal processing.

Power consumption is 8 mW under normal operating conditions but this can be further reduced to 1 mW, using its *sleep* mode, when the device's *mode* pin is grounded. The AD7883, with operating temperatures from −40 to +85°C, is available in 24-pin DIP and SOIC packages. Prices start at $14 in 100s.

OP-295 Dual Op Amp: The OP-295† is a dual CBCMOS (complementary-bipolar-CMOS) operational amplifier specified for operation on +3.0-volt supplies (it is also specified for ±15-volt and +5-volt supplies). It features low power dissipation, typically 480 μW, with a single +3-volt supply. Its output voltage can swing rail to rail (+0.002 V to +2.9 V), and the input common-mode range is from 0 to 2.0 V.

Its performance specs are excellent, with 110 dB typical, 90-dB minimum common-mode rejection over the entire common-mode-voltage and operating temperature ranges. It has maximum offset voltage of 500 μV, 100 μV typical, and 1 μV/°C drift, 20-nA maximum bias current and ±3-nA maximum offset current, with large-signal voltage gain of 750,000 V/V.

It will drive a 10-kΩ load with a slew rate of 0.03 V/μs; its small-signal gain-bandwidth is 75 kHz, with an 85° phase margin. The OP-295 is available in both 8-pin mini-DIP and SOIC packages, and operates at temperatures from −40 to +85°C. Prices start at $1.98 in 1000s.

A PRACTICAL 3-V DATA-ACQUISITION SYSTEM

The circuit in Figure 2 shows a complete 4-channel data acquisition system using the above devices (Bypass capacitors are of course recommended but are not shown in order to reduce clutter). The circuit operates as follows:

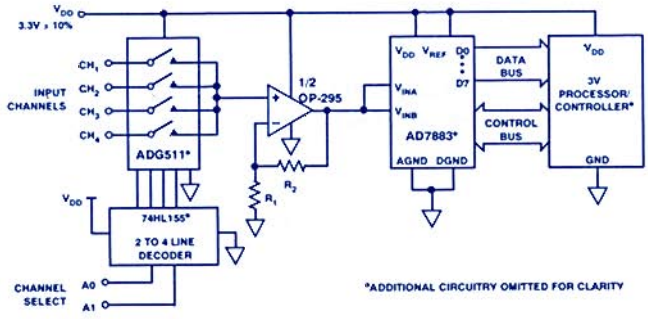


Figure 2. Four-channel data-acquisition system using a +3-volt supply.

The ADG511 quad analog switch and the 74HL155 two-to-four-line decoder together constitute a four-channel multiplexer. One of four input channels, CH1 to CH4, is selected, as determined by the levels of the channel-select inputs, A0 and A1. The signal on the selected channel is amplified and buffered by the OP-295, with a gain of $[1+R_2/R_1]$. The amplified signal is applied to the AD7883 ADC where it is sampled and converted to a 12-bit digital word.

*Use the reply card for technical data. Circle 7
†Use the reply card for technical data. Circle 8

The ADC is configured for an analog input range 0 to $+V_{REF}$. Because V_{REF} in this simple example is connected to VDD, the input range is 0 to +3 V. For greater accuracy, a stack of two AD589 1.235-V two-terminal references§ (with an appropriate series resistor, say 250 Ω) will provide a 2.5-volt range; alternatively, the other channel of the OP-295 dual op amp can be used to scale a single AD589's voltage up to +3 V. The gain resistors, R1 and R2, should be chosen to amplify the input signal sufficiently to utilize the entire dynamic range of the ADC—but without clipping.

The overall system bandwidth is limited by the operational amplifier, since the multiplexer and the ADC both have much higher signal bandwidths. There is usually a tradeoff between bandwidth and power consumption in amplifier design. Low-power amplifiers tend to have limited slew rates, which will limit the system bandwidth. The OP295 slews at 0.03 V/μs when powered with a +3-volt supply. This limits the full-power bandwidth to about 1 kHz, with a small-signal gain-bandwidth of 75 kHz. The 1-kHz full-power bandwidth is often not an important limitation; the required bandwidth may be considerably lower. For example, many transducers have bandwidths below a few hundred hertz.

Discussion of Test Results

Figure 3 shows the results of an evaluation of the circuit of Figure 2, using an FFT test. The input signal frequency was 1.11 kHz and peak-to-peak amplitude was 2.2 V. Signal-to-noise-plus-distortion was measured at 67 dB over the 30.7-kHz band, with total harmonic distortion of −72 dB (principally 2nd and 3rd). The FFT plot is shown in Figure 3. Lower input frequencies will yield better THD performance, since the distortion caused by slew-rate limiting will be reduced or eliminated.

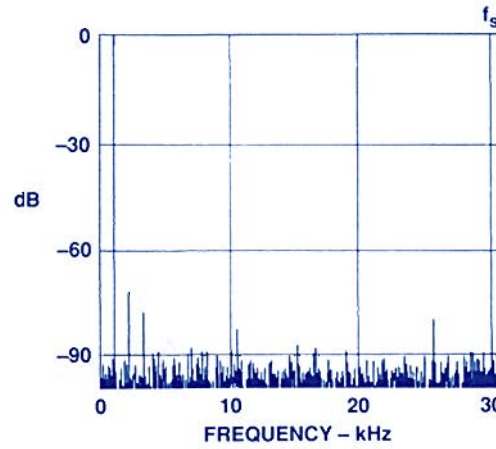


Figure 3. Response spectrum for 1.11-kHz sine wave sampled at 61.44 kHz.

The authors would like to acknowledge the work of Sean O'Leary in building and testing the data-acquisition circuit.

§The AD589 1.235 voltage reference has long been in our catalog (*Analog Dialogue* 14-1, 1980, p. 14), but it is worth taking a new look at it in the 3-volt era. A 2-terminal device, it can be thought of as a high-precision Zener diode. It will work on currents as low as 50 μA, with a dissipation of 60 μW. It has a dynamic impedance of 2 Ω maximum at 500 μA and a range of guaranteed tempcos down to 10 ppm/°C. Two stacked devices provide both a 2.5-volt reference and at the same time an artificial "ground" at +1.235 V for bipolar signal swings. The AD589 is available in metal can and SOIC and for 0 to +70°C and −55 to +125°C temperature ranges. Prices start at $1.25 in 100s. For technical data, use the reply card. Circle 9

Op Amps in Line-Driver and Receiver Circuits

Part 2. Audio applications

by Walt Jung and Adolfo Garcia

INTRODUCTION

The first article in this series (*Analog Dialogue* 26-2),* covering general line driving and buffer design considerations, gave examples of *video* line-driver and -receiver designs. In this article, we consider *audio* line drivers and receivers. The general techniques are still germane, in particular the amplifier tables and buffer design/selection guidelines. Capacitive load isolation is also important to audio drivers; long transmission lines appear capacitive because audio transmission systems do not tend to use terminated transmission lines. In general, the "housekeeping" rules on layout and bypassing are also strongly recommended for practical audio circuits of any type, especially drivers (and were followed for the examples in this article).

Transmitting audio signals between various components usually involves some form of tradeoff. For highest performance, fully differential or balanced transmission systems are best at rejecting low frequency and r-f noise. Figure 1 is a block diagram of a typical audio system using differential transmission. In concept, a variety of input/output coupling schemes are available for a balanced transmission system; they will be discussed briefly.

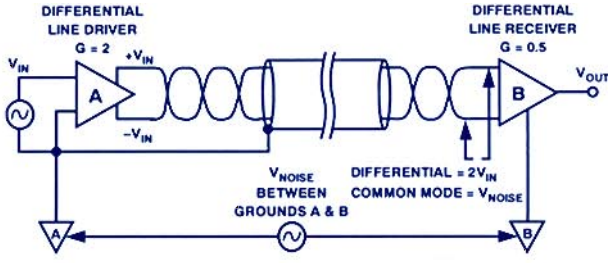


Figure 1. Audio balanced transmission system.

Transformers [1]-[4] have been a traditional input or output audio line-coupling element. While unexcelled in certain areas, they have well-known problems: noise pickup, poor frequency response, distortion, and limited operating level—problems that can be mitigated to some degree (often at fairly high cost).

The transformer's outstanding virtue is its ability to isolate galvanically voltages up to its windings' breakdown potential; signals can be transmitted between circuits with hundreds of volts of potential difference, a feature not easy to achieve with solid-state circuits. Quite high common-mode rejection (CMR) is also available, >100 dB over the audio range, less at high frequencies.

Figure 1 can use either transformer or active coupling to the line. The goal for either approach is to reproduce the input signal, V_{IN}, at the output, while rejecting noise between grounds A and B by 80-100 dB. A typical unity gain design uses a line drive of $\pm V_{IN}$ and a receiver gain of 1/2, to maximize receiver CMR.

AUDIO LINE RECEIVERS

A major purpose of this circuit and all line receivers is to reject common-mode noise, as might be picked up on a twisted-pair transmission line. A brief review of the topologies and pros and cons of active audio line receivers helps in understanding their evolution. The classic single-op-amp, 4-resistor subtractor circuit of Figure 2 can act as a differential amplifier. When the resistor ratios provide gain, the circuit is known as an instrumentation amplifier (IA). Some of today's IC audio line receivers, based on feedback circuitry, are direct descendants of this circuit. [5]-[9]

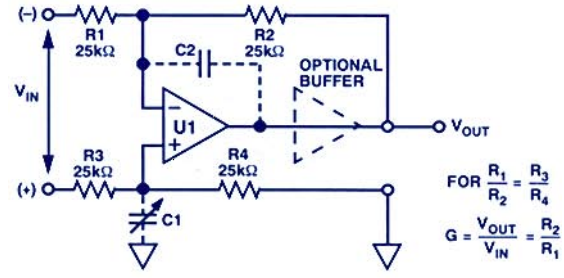


Figure 2. Simple line-receiver topology.

The simple line receiver

The circuit of Figure 2 is simple; the minimum ingredients are four matched film resistors and a good audio op amp. While it works functionally, its degree of common-mode rejection (CMR) may be problematical. The performance of such bridge-based difference amplifiers depends critically upon resistor-ratio matching—including source impedances in series with R1 and R3. The amplifier also contributes error, but with a high-quality op amp, noise rejection is limited by ac & dc bridge unbalance.

Selecting four discrete resistors from a same-vendor-same-batch lot, to ratio-match within 0.1%—or (more likely) using a purchased thin-film network with a 0.1% specified mismatch—results in CMR of 66 dB. In general, the worst-case CMR of this type of circuit (amplifier CMR ≥100 dB):

$$\text{CMR (dB)} = 20 \log \frac{1 + R_2/R_1}{K_r}$$

where K_r is the net ratio tolerance in fractional form.[5] Clearly, for high and stable noise rejection with temperature tracking, thick- or thin-film resistors integrated on a single substrate with ratio matching to within 0.01% (from vendors such as Caddock and Vishay-Ohmtek) are preferred to selected individual resistors.

The Figure 2 topology is most effective when the resistors and amplifier are made simultaneously in a single monolithic IC. The Analog Devices 8-pin SSM-2141 and SSM-2143† are such ICs, designed and characterized as low distortion, high CMR audio line receivers with net gains of 1.0 (SSM-2141), and 0.5 (SSM-2143). The SSM-2141 has the same resistance values as in Figure 2, while the SSM-2143 uses 12-kΩ/6-kΩ resistors.

Amplifier protection is inherent in two ways: the input common-mode voltage (CMV) in the unity-gain case is halved at the amplifier inputs (and can be further reduced by resistors to ground), and the series resistance limits fault currents due to excessive

*Use the reply card. Circle 18 for *Analog Dialogue* 26-2, 19 for the article reprint.

†Technical data for the amplifiers mentioned in this article can be found in the *1992 Amplifier Reference Manual*, available at no charge. If you need a copy circle 10

CMV. Receiver circuits not needing input resistors may call for input resistors anyway for protection in practical circuitry.

Figure 2's working CM input range is $[1+(R_3/R_4)]\times V_{CM(U1)}$, and the differential input resistance is $R_1 + R_3$. Gain of the circuit isn't easily changed, because of the matched R-ratios.

For wideband audio uses, the bridge *impedance*-ratio match needs to be maintained for ac, to achieve flat CMR with increasing frequency. Capacitances at the R_2/R_1 and R_4/R_3 nodes need to be balanced. This is best achieved with very low and/or balanced parasitic capacitances at C_1-C_2.

Implementing the simple line-receiver function

For adequate input impedance, these receivers typically use input resistance ≥20 kΩ. With a well matched resistor network and low- or balanced parasitic capacitances, suggested amplifiers are the AD711 and AD744 (singles), and the AD712, AD746, OP-249 and OP-275 (duals). With 10-25 kΩ resistances, extremely low amplifier voltage noise is not a critical requirement, but high slew rate (SR) and husky output drive permit high amplitude levels, clean high-frequency response, and 600-Ω loads.

For circuits such as these, that resistively load the source, the line and source resistances, if unbalanced, can compromise CMR. For example, a mismatch of 2.5 Ω can easily occur in wiring; if it is not balanced out, CMR can be degraded to 86 dB. These circuits behave best when the sources are balanced and low-impedance.

Other issues with the simple line receiver

The circuit of Figure 2 has symmetry of a sort, but it is not really balanced. If a balanced pair of input voltages, $+V_{IN}$ and $-V_{IN}$, are applied to the two inputs, the currents in the two legs are different. Here, the current in the R3 leg is $V_{IN}/50$ kΩ and the current in the R_1 leg, because of the op-amp feedback action, is $[-V_{IN} - V_{IN}/2]/25$ kΩ $= -3V_{IN}/50$ kΩ, *three times as much*. Thus, the inputs load the source and the connecting lines differently. If the source is a transformer winding, the circuit will unbalance the line, driving the minus-input side to virtual ground.

Ideally, an audio line receiver should exhibit equal ac loading at the two inputs. With the simple line receiver of Figure 2, this goal is not met. Nevertheless, for a grounded symmetrical source and line pair, with a single receiver, loading of the source resistance will produce a gain error, but the asymmetrical current will not substantially affect the CMR because feedback will compensate for the greater voltage drop on the R1 side. But, in systems with numerous balanced transmission line pairs, the input current imbalance may be more serious; associated fields will not cancel as they do for completely balanced loading. Thus there is potential for crosstalk impairment in such systems.

While not optimum in large systems, the simple line receiver is nevertheless useful in more modest situations. With resistances R_1-R_3 relatively high (20 kΩ or more), it is quite adequate for small-scale or confined systems where I/O lines are relatively short or few in number—or are not cabled. Devices like the SSM-2141 and SSM-2143 serve well as efficient single-IC solutions.

A balanced form of line receiver

Birt, of the BBC, analyzing the simple line receiver topology, has described a balanced form[4]: in Figure 3, U1 uses an identical 4-resistor network, but the unity-gain inverter, U2, drives R4's previously grounded reference terminal at $-V_{OUT}$. This equalizes the input currents in the ± input legs and provides a choice of a balanced push-pull output with gain of R_2/R_1 or a single-ended output of either polarity with gain of 1/2 $[R_2/R_1]$ (one-half that of the Figure 2 circuit). Existing line receivers can be converted to the balanced topology by adding an appropriate inverter, U2, and doubling the gain ($R_2/R_1 = R_4/R_3 = 2$) if necessary. The common-mode range of this circuit is the same as for Figure 2, but common-mode rejection at V_{OUT} (or $-V_{OUT}$) is about doubled with all resistances nominally equal. The inverter resistance ratio, R_6/R_5 affects balance—but not CMR.

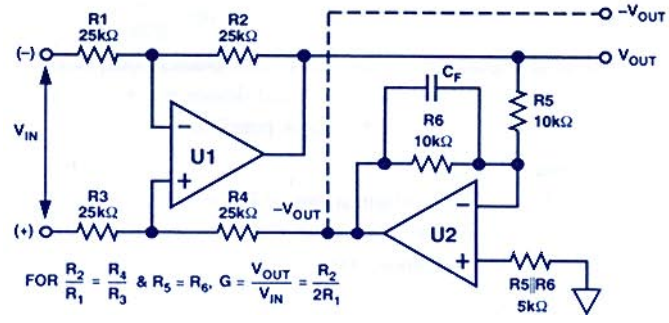


Figure 3. Balanced line receiver using push-pull feedback path.

Other balanced line receivers

Why not use an instrumentation amplifier [5-8] as a line receiver? Conventional high-input-impedance instrumentation amplifier circuits (including single-chip in-amps) can easily achieve the goal of fully balanced input loading. Too, they may specify high CMR—but generally at low frequencies. They may not be desirable for other reasons. For example, the input resistors of circuits like Figure 2 reduce common-mode voltage and limit fault currents, a necessary input-protection consideration in many real world audio systems. To add matched attenuators ahead of an in amp for this purpose degrades performance and adds cost.

An "all inverting" balanced line receiver

Figure 4, using only inverting amplifiers, can be configured for high CMV range and input resistance. The CMR of this circuit is limited essentially by the ability to match resistance ratios, since the amplifiers' CMRs are irrelevant. The maximum input voltage the circuit can handle is limited by the output range of U1, so R_1/R_2 can be increased to deal with higher common-mode input voltages. The differential input resistance is R_1+R_3.

Unlike the others, the gain of this circuit can be adjusted with a single resistance, R_5, without disturbing the CMR. Gain can be flexibly adjusted to values both greater and less than unity. As shown, the drive is a balanced signal, but note that it can be driven with single ended sources at either the (+) or the (−) terminal. Multiple inputs can be summed, by adding additional ratio-matched input-resistor pairs. This example shows a gain of 0.5.

In this improved version of the otherwise well-known circuit [5]-[8], phase lead compensation enhances high-frequency CMR. R_4 is shunted by a low capacitance (driven through an attenuator), chosen to compensate for the lag through U1; it maximizes phase matching of the ±CM signals at U2. The attenuator (R_6-R_7) can be used to avoid extremely low capacitance values. Its nominal division ratio is approximated by:

$$K_c = \frac{1}{2\pi\,\mathrm{BW(U1)}\,R_4\,C_1}$$

where K_c is the division ratio of R_6-R_7. For this example, with BW = 5 MHz (the closed-loop bandwidth of U1), K_c is about 0.6, providing an effective C_c of about 3 pF. Circuit parasitics,

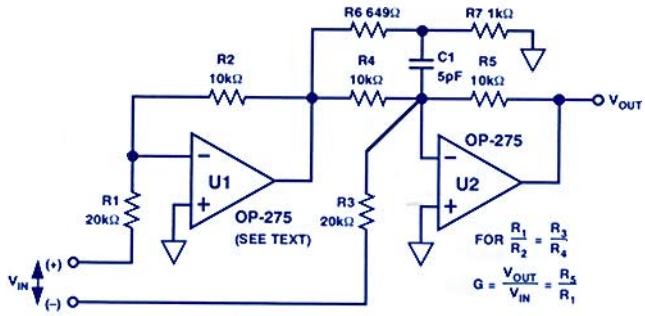


Figure 4. Dual-Inverter line receiver.

loading effects, and part variations make this inexact; but, once nominal compensation for a given layout and device is achieved, a 30-dB improvement in CMR at 10 kHz is possible.

Line-receiver performance

The balanced line receiver configurations of Figures 3 and 4 were tested for CM performance, with the common conditions of G = 0.5, V_s = ±18V, a balanced 600-Ω source, and a 10-V rms 20 Hz to 50 kHz input sweep, with filter bandwidth of 80 kHz. Figure 3 was implemented with an SSM-2141 and an OP-275 inverter, with C_f = 68 pF. Figure 4, implemented with an OP-275 and a resistor network matched to 0.005%, is shown with the phase-lead-network values for best high-frequency CMR.

The excellent results for both circuits are shown in Figure 5. CME is −100 dB or less for frequencies up to 1 kHz, with little sensitivity to source impedances of 50 Ω to 600 Ω (not shown). The Figure 4 topology offers better results at the higher frequencies, perhaps due to the trimming technique used (not applicable to Figure 3). The worst-case CM errors are still less than −80 dB at 10 kHz, still very good for an untrimmed circuit. CM data for Figure 4 were also taken for the other devices noted above, with good-to-excellent results, but the OP-275 is illustrated here because of the generally higher output drive. THD+N data, taken on both circuits, was mostly dominated by the noise floor of the circuit, at about 100 dB below 1 V rms.

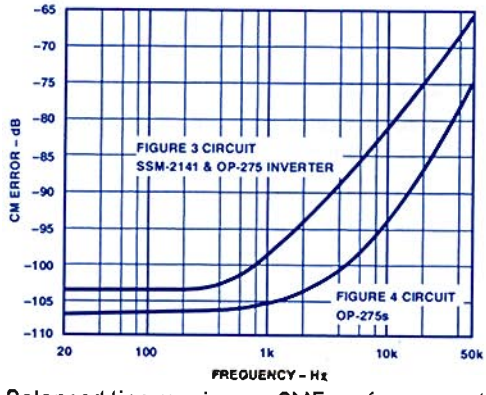


Figure 5. Balanced line receivers—CME vs. frequency (G=0.5. V_S = ±18 V, R_S = 600 Ω).

AUDIO LINE DRIVERS

Audio line driver principles do not differ substantially from those discussed in the first of this two-part series (*Analog Dialogue* 26-2). Indeed, many of the op amps mentioned as video drivers and/or buffers also do well for audio. Types already popular for audio include the AD845, AD846, AD847 and OP-42, while newer types such as the AD797, AD817, AD818 and OP-275 should upgrade performance in specific audio applications. The circuits shown here use series resistance to isolate capacitive loads; with 600-Ω lines, the compensatable gain error is <1 dB.

Single-ended line drivers

Single ended audio driver circuitry can be built using Fig. 2 of Part 1 as a starting point; indeed that circuit example (with appropriate op-amp choice and gain scaling) can serve well as an audio driver. Using the AD845, the circuit has low loaded distortion with high slew rate (SR) and output current.

A wide-dynamic-range ultra-low-distortion driver

Single-ended line drivers may seem simple; but, when pushed to their performance limits in dynamic range and distortion, they require careful device choice. One answer is the AD797, a new op amp (see page 18) with typical gain of 146 dB, <1 nV/√Hz noise, and a unique 50-mA distortion-cancelling output-stage design (patent pending).[11] Its buffered single-stage topology also results in improved bandwidth (450 kHz for gain of 1000), phase margin, and settling time (800 ns to 16 bits).

Figure 6 shows it in an application combining line driving with amplification (gain of ×10). Internally compensated to be stable at unity closed-loop gain, it delivers optionally improved performance at higher gains with a 50-pF capacitor connected between the output and its distortion-cancellation terminal, pin 8. The values for R1-R2 are recommended for best noise (select gain/source resistors with care; high values will degrade noise performance). For a 600-Ω load, typical THD in this application is −115 dB at 20 kHz at 3-V rms output, with ±15-V supplies—and the circuit's −3-dB bandwidth is 6 MHz.

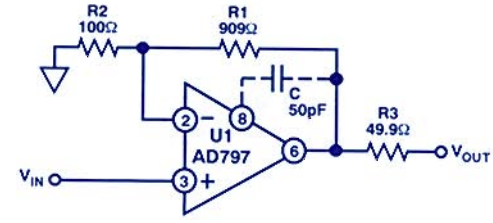


Figure 6. Ultra-low distortion ±50-mA driver.

A composite line driver

Another useful circuit technique [10] combines two amplifiers in a closed loop; the composite device forms a high-performance line driver, capitalizing on their individual strengths. In Figure 7, a

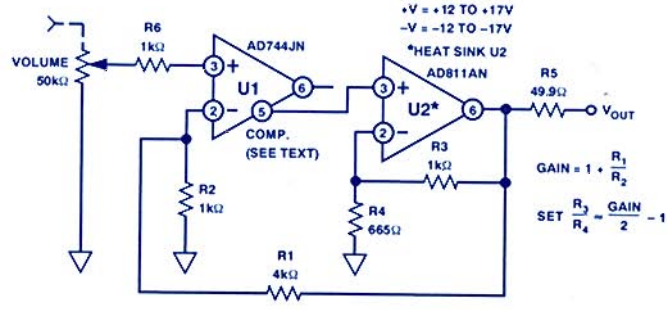


Figure 7. A low-distortion-composite ±100-mA line driver.

low-distortion line driver combines the high input impedance of a FET-input IC and the power of a high-performance op amp that can deliver >100 mA. Here, the AD744's low bias current minimizes offset error over the range of adjustment of a 50-kΩ volume control. The wideband high-current AD811, fed back for gain of 2.5, boosts both current and voltage (i.e., power); it can drive 150-Ω lines with excellent linearity.

In an unusual connection (unique to the AD744), U1's output is (yes!) left open; pin 5 (the compensation terminal) drives U2's

high-impedance input for increased overall phase margin. The gain-bandwidth and SR of U1 are boosted by the closed-loop gain of U2, an AD811 high-performance transimpedance amplifier. Though primarily intended for video, its high output-current drive capability enhances linearity in audio line driving.

As a non-inverting feedback amplifier, the circuit has an overall gain determined by R_1 and R_2, in this case the gain is 5× (i.e., 14 dB). The gain of the local loop around U2, determined by R_3 and R_4, reduces U1's output voltage drive and enhances overall stability. R_3 has the specified preferred value for U2 stability. Performance is rather good: for a typical audio load of 600 Ω —light loading for this circuit—THD+N at an output level of 5 V rms is of the order of 0.001% for frequencies below 20 kHz. For supply voltages of ±12 V or more, a clip-on heat sink is recommended for U2, as suggested in the earlier article.

Two contrasting balanced differential line drivers

"Inverter-follower" line driver

A balanced output signal, $\pm V_{IN}$ with respect to common, can be derived from an input, V_{IN}, by operating on it with side-by-side unity-gain amplifiers of opposing sense. The differential output voltage is $2V_{IN}$ (as in Figure 1). Other values of gain could be used to provide the amplification needed to the desired line level.

This "inverter/follower" driver is easily accomplished with a dual op amp, such as the OP-275, and an 8 × 20-kΩ film or discrete resistor network (Figure 8). U1A provides a gain of −1, and U1B operates at a gain of +1. The balanced differential output to the line is $2V_{IN}$, with a 100-Ω differential output impedance.

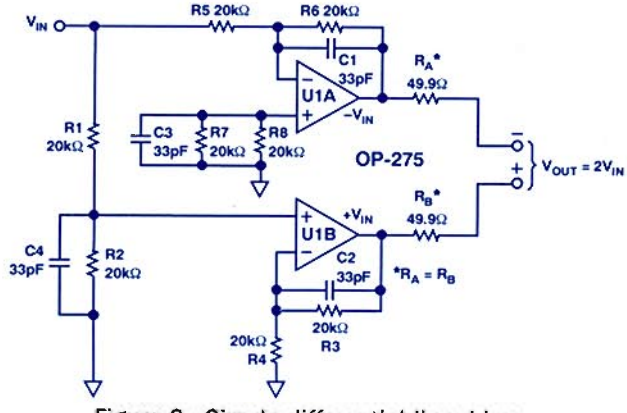


Figure 8. Simple differential line driver.

Readily available equal-value gain resistors are used around the U1 sections to provide symmetrical loading at the amplifier input terminals and matched noise gains for similarity of bandwidths and dynamics. Capacitors C1-C2, which cause the response to roll off at ultrasonic frequencies, enhance dynamic stability. This circuit provides good performance with simplicity and low cost, needing only U1, a resistor network, and 4-6 passive components.

A caveat should be kept in mind. Though the push-pull output circuit is simple and can achieve high performance in a limited class of systems (high-impedance, differential-input receiver circuits), some line destinations may incur problems. The outputs are not truly differential and floating—unlike a transformer, neither side can behave properly when grounded. The 49.9-Ω series resistors limit fault currents. Even though half the signal may be lost, damage is not likely.

Cross-coupled differential line driver

A more versatile gain-of-2 differential line driver uses a pair of cross-coupled differencing op amps. The circuit compares the voltage across the load with 2× the input voltage and ideally provides whatever values of current are necessary to maintain equality, regardless of the actual common-mode output voltage. Like a transformer, it works, even with grounded loads.[12]

Figure 9 shows a block diagram of the monolithic SSM-2142 balanced line-driver circuit. Inverter A1 provides a push-pull input of $2V_{IN}$ to the cross-coupled differencing amplifiers, to be compared with the differential load voltage fed back by the *sense* terminals. The *force* outputs, through 50-Ω isolating resistors, are driven to produce the correct voltage at the *sense* terminals.

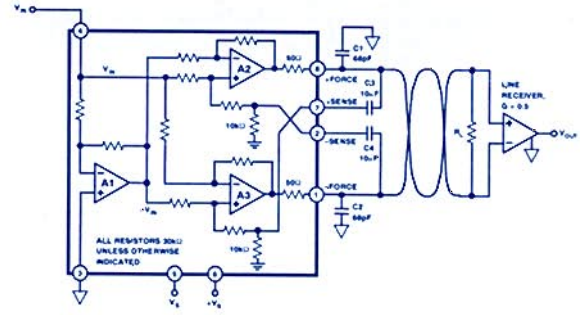


Figure 9. SSM-2142 differential driver system.

The SSM-2142, housed in an 8-pin mini-DIP, is designed to work into a 600-Ω load. In the simplest use, it is simply strapped with the appropriate force/sense pins tied together. Small capacitors (C1,C2) preload the IC for stability against varying cable lengths. Where dc offsets are expected, the optional 10-μF capacitors (C3,C4) may used to allow the outputs to maintain ac feedback over the audio band; the capacitors should be non-polar types unless the offset polarity is known.

In a system application, the SSM-2142 is used with a complementary gain-of-0.5 receiver, (an SSM-2143 or one of the other receivers mentioned). The circuit in Figure 9 comprises a complete unity-gain single-ended-to-differential-to-single-ended transmission system. Typical THD+N from 20 Hz to 20 kHz at 10-V rms output, driving 600 Ω, is of the order of 0.003% or less.

The authors acknowledge helpful comments from David Birt, of the BBC (ret.) and Neil Muncy, of Neil Muncy Associates.

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The New Op Amps—1

Two Op-Amp Types Combine Precision and Wide Bandwidth

AD797 has lowest distortion, low offset & drift, ultra-low noise; Dual OP-285 includes low bias current & supply current, low cost

These two high-performance operational amplifiers with excellent dc and dynamic specs offer a win-win choice. Pick the **AD797*** for a no-compromise approach to near-ideal performance; choose the dual **OP-285*** where high speed and dc performance must be combined for multiple channels at lowest cost. Table 1 shows—in a nutshell—their similarities and differences.

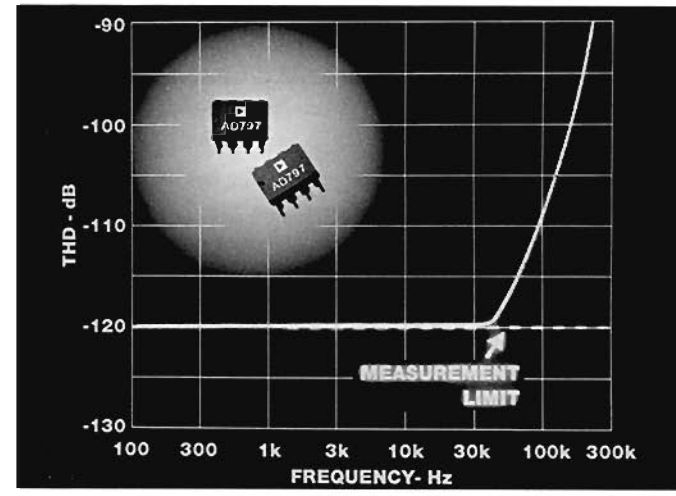
The OP-285's single chip features two identical precision laser-trimmed operational amplifiers employing the Butler front end (Analog Dialogue 26-2, 1992, p. 11). This patented design combines the accuracy and low-noise performance of bipolar transistors with the speed of JFETs. The resulting amplifier has high slew rates, low offset, and good noise performance at low supply currents (5 mA max over the operating voltage and temperature ranges). Bias currents are also low compared to bipolar designs. A useful component of high-speed instrumentation- and dc-coupled audio systems, the OP-285 may be used in such applications as instrumentation amplifiers, ramp generators, line drivers, current pumps, and filters.

Salient specifications, in addition to those noted below, include long-term offset-voltage of 300 microvolts maximum. Internally compensated, its unity-gain bandwidth is 9 MHz, with a 62° phase margin. Distortion as a unity-gain follower is typically −104 dB at 1 kHz, with 2-kΩ resistive load. The OP-285, specified for operation over temperatures from −40 to +85°C, is available in 8-pin plastic DIP and SOIC packages.

Table 1. The AD797 and the OP-285—specs in brief

	AD797A/S	AD797B	OP-285
Supply voltage range	±5 to ±18 V		±4.5 to ±22 V
Supply voltage	±5 V, ±15 V		±15 V
Offset voltage, max, 25°C	80 μV	40 μV	250 μV
max over temperature'	125/180 μV	60 μV	600 μV
Bias current, max, 25°C	1.5 μA	0.9 μA	350 nA
max over temperature	3.0 μA	2.0 μA	400 nA
Offset current, max over T	600/700 nA	300 nA	±100 nA
CMR, min over temperature	110 dB	114 dB	80 dB
Open-loop gain, min over T (2 kΩ)	1 V/μV†	2 V/μV†	175 V/mV
(R_L = 600 Ω)	1 V/μV†	2 V/μV†	200 V/mV typ, 25°C
Voltage noise, 0.1 Hz to 10 Hz,	50 nV typ†		
p-p spectral density, typ 1 kHz	0.9 nV/√Hz†		6 nV/√Hz
Slew rate, typ (1 kΩ load)	20 V/μs†		22 V/μs (2 kΩ)
Settling time to 0.0015% (16 bits)	800 ns typ†		
to 0.01%			750 ns typ
Total harmonic distortion, typ	−120 dB		−104 dB
Price (1000s, 8-pin SOIC, $US)	$3.36 (A)	$5.04	$1.90

†Specs apply for ±15-V supply.



The **AD797** offers the industry's best combination of voltage noise and distortion, with noise spectral density of 0.9 nV/√Hz at 1 kHz (1.2 nV max), remaining flat to beyond 8 MHz, and maximum total harmonic distortion (THD) of −110 dB (−120 dB typical) at audio bandwidths (20 kHz). In wideband voltage noise, the noise is equivalent to that of a 50-Ω resistor; thus the AD797 is optimal for use in low-impedance circuitry (source resistances less than 1 kΩ).

Its excellent dynamic specifications include gain-bandwidth of 8 MHz at gain of 10, increasing to 110 MHz at gain of 1000 (and can be further increased to 450 MHz, using an external decompensation capacitor). The low distortion specification results from a patented on-chip distortion-cancelling circuit, which also produces very high open-loop voltage gain, 2 V/μV max, 7 V/μV typical, with ±10 V output into a 600-Ω load—over temperature. At 20 kHz, the open-loop gain is still 14 V/mV maximum, 20 V/mV typical.

Its near-ideal voltage specifications include maximum: offset (B grade) of 40 μV at 25°C, 60 μV over temperature, and drift of 0.6 μV/°C. However, bias current is 2 μA max over temperature (250 nA typical), with max offset of 300 nA over temperature (120 nA typical) and typical current noise of 2 pA/√Hz.

The excellent combination of voltage noise, distortion, and bandwidth specifications, and the fast settling to 16 bits, as well as its 30-mA minimum output-current (50-mA typical) and the 80-mA short-circuit current, make it useful in a variety of applications, including preamplification and buffering for a wide range of equipment, such as FFT and spectrum analyzers (low distortion), audio and seismic applications (low noise and distortion), ultrasound (low noise & distortion, high output drive). Other uses might include low-noise front ends for infrared detection, automatic test, and ac instrumentation.

The AD797 draws 10.5 mA maximum at ±5 V and ±15 V. It is available in two −40 to +85°C grades (A,B) and a −55 to +125°C grade (S). The A and B grades are available in 8-pin Plastic DIPS and SOICs.

The AD797 was designed by Scott Wurcer in Wilmington, MA; the OP-285 was designed by James Butler in Santa Clara, CA.

*Use the reply card for technical data. Circle 12 for AD797, 13 for OP-285

The New Op Amps—2

Four New Wideband Op Amps for Video, Imaging, & Much More

AD810: High slew rate & $\overline{\text{DISABLE}}$
AD817: High speed, low cost
AD818: Best price/performance
ADEL2020: 2nd source, 1st choice

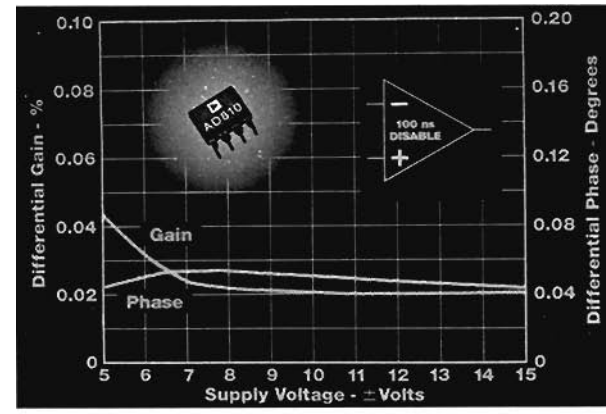
These video op amps provide optimal price-performance in a wide range of video-speed applications. For example, the **AD817*** and **AD818*** will drive heavy current loads and are specified for operation on +5-volt single supplies, as well as ±5-volt and ±15-volt dual supplies. The AD817 will drive large values of capacitive load stably. The **AD810***—and the ADEL2020*—have a $\overline{\text{DISABLE}}$ control input to initiate an energy-saving power-down mode or provide a multiplexed channel (100-ns turn-off time, guaranteed break-before-make). The ADEL2020, which has an extant second source, will bring improved performance to existing sockets (both 8-pin mini-DIP and 20-pin SOIC) with less power drain—and at a lower price.

The **AD810** is a current-feedback video operational amplifier, compatible with composite and high-definition TV systems. Its flat frequency response (typically within 0.1-dB up to 30 MHz) at gains of +2, and its differential gain and phase of 0.02% and 0.04° (NTSC) make the it ideal for broadcast-quality video systems. This performance is specified with a 150-Ω load (a 75-ohm back-terminated cable).

The AD810 is ideal for power-sensitive applications, such as portable video cameras, with its low power-supply current of 8.0 mA max. The *disable* feature can be used to reduce the supply current to typically 2.1 mA when the amplifier is not in use, to conserve energy. In addition, the AD810's performance is specified for both ±15-volt and ±5-volt levels of V_S, to make possible further energy savings.

Table 1. Video op amp specs in brief

	AD810	AD817	AD818	ADEL2020
Supply voltage range, V, max	±2.5 to ±18	(+5 to ±18)		±3 to ±18
Supply voltage specs published, V	±5, ±15	+5, ±5, ±15	+5, ±5, ±15	±15
Feedback type	Current	Voltage	Voltage	Current
Bandwidth, 0.1 dB, MHz (G), typ	30 (+2)	40 (+1) min	55 (+2)	25 (+2)
3 dB, MHz (G), typ	80 (+1)	45 (GBW) min	130 (+2)	90
Slew rate, V/µs, typ	1000	350	500	500
Settling time to 0.01%, ns typ	125	70	80	—
to 0.1%, ns typ	50	45	45	60
Differential gain, %typ (max)	0.02 (0.05)	0.04 (0.08)	0.01 (0.02)	0.02
Differential phase, °typ (max)	0.04 (0.07)	0.08 (0.1)	0.05 (0.09)	0.04
Offset (drift), mV max T (µV/°C typ)	7.5 (7)	3 (10)	3 (10)	10 (7)
Output current, mA min	45	50	50	30
Short-circuit, mA typ	150	90	90	150
Supply current, mA max	8	7.5	7.5	10
Power down (Disable), mA max	2.8	—	—	3.0
Voltage noise, 1 kHz, max, nV/√Hz	2.9	15 (10 kHz)	10 (10 kHz)	2.9
Price (1000s, DIP or SOIC, $US)	$2.08	$1.52	$1.69	≤$1.99



With its bandwidth of 80 MHz typical as a unity-gain follower, the AD810 works well as an ADC or DAC buffer in digital video systems. As a transimpedance amplifier, it can maintain wide bandwidth over a range of gains, and its low noise of 2.9 nV/√Hz permits it to handle wide-dynamic-range signals.

The AD810 is available in both A (−40 to +85°C) and S (−55 to +125°C) versions. The A is available in 8-pin mini-DIP and SOIC packages; the S is housed in Cerdip.

The **AD817** is optimized for video applications requiring stable operation when connected for unity gain. In applications such as ADC buffers and line drivers† it simplifies the design task with its unique combination of 50-mA minimum available output current and the ability to drive large capacitive loads stably without greatly affecting signal integrity.

Capable of operating over a range of ±2.5 to ±18 V with dual supplies, or +5 to +36 V with a single supply, the AD817 is specified for operation with +5-, ±5-, and ±15-volt supplies. It is available in 8-pin mini-DIP and SOIC packages.

The **AD818**, with the same supply voltage range as the AD817, is similarly available with specifications for both +5-volt single-supply and ±5-V and ±15-V dual-supply operation. It is optimized for video applications calling for gains of magnitude equal to or greater than +2 or −1. With its low differential-gain and -phase errors, ability to work on single supplies as low as +5 V, low power drain and high output drive, it is ideal for cable-driving in video cameras and professional video equipment.

Its useful characteristics for video include such typical performance specs as flat frequency response (within 0.1 dB) to 55 MHz, differential gain and phase errors of 0.01% and 0.05°, and 50 mA of output current. Its 130-MHz 3-dB bandwidth and 500-V/µs slew rate are highly desirable for applications in such equipment as video monitors, cable TV, color copiers, image scanners, and fax machines. The AD818 is available in 8-pin plastic mini-DIP and SOIC packages.

The AD810 and ADEL2020 were designed by Dave Whitney—and the AD817 & AD818 were designed by Alex Gusinov and Mike Gianino at Wilmington, Mass.

*Use the reply card for technical data. Circle 14 for AD810, 15 for AD817, 16 for AD818, 17 for ADEL2020

†For an in-depth discussion of video line drivers, and the application of AD810, AD817, AD818, and other amplifiers, in these circuits, see the article, "Op amps in line-driver and -receiver circuits: Part 1. Video applications," by Walt Jung in Analog Dialogue 26-2 (1992). Use the reply card. Circle 18 for Analog Dialogue 26-2, 19 for the article reprint alone.

The New Op Amps—3

Low-Noise, Low-Drift Precision Op Amps for Instrumentation

AD795 has low noise, bias current, and drift; Dual OP-213 is specified for both ±15 V and single supply, +5 V

These new amplifiers are designed to handle two widely differing instrumentation problems: the **OP-213*** dual amplifier for instrumenting low-voltage amplification in single-supply systems where low drift and voltage noise are critical requirements (and multiple channels may be needed)—and the **AD795*** for high-impedance voltage and current measurements with low drift and noise in low-cost *plastic* DIP and SO packages. Salient specs in brief for available versions are compared in the Table.

The **OP-213** dual operational amplifier features the lowest noise (120 nV p-p, 0.1 to 10 Hz) and drift (1 μV/°C) among single-supply amplifiers. This is an important virtue for amplifiers used in self-calibrating precision measurement systems; while such systems can correct for gain- and system offset errors, temperature drift and noise is a considerably more difficult matter. Optimized for these parameters, the OP-213 can be used to advantage by combining its superior analog performance with the system's digital correction. Many systems using internal calibration operate from unipolar supplies, usually either +5 or +12 volts. The OP-213 is designed to maintain low noise and precision performance while operating with single supplies from +4 V to +36 V. Figure 1 shows an application as an ultra-low-noise single-supply instrumentation amplifier.

Dynamic performance is reasonable, including unity-gain stability, typical gain-bandwidth product of 3.4 MHz, and slew rate in excess of 1 V/μs. Its noise spectral density at 1 kHz is only 4.7 nV/$\sqrt{\text{Hz}}$. Input common-mode range and output range are from within millivolts of the negative supply (ground in single-supply operation) to within 1 volt of the positive supply. The output can both sink and source current and includes single-supply specifications for 600-ohm loads. As noted, E and F versions are available for −40 to +85°C operation. Packages include plastic DIPs, C-DIPs (E), and 8-pin SO.

Table 1. Specifications in brief

	OP-213E	OP-213F	AD795J	AD795K
Supply voltage range, V,max	+4 to ±18		±4 to ±18	
Supply voltage, V	±15 (+5)	±15 (+5)	±15	±15
Offset voltage, μV,max, 25°C	100 (150)	250 (300)	500	250
max over temperature'	150 (225)	325 (375)	1000	400
drift, μV/°C,max	0.8 (1.0)	1.5 (1.5)	10	3
Voltage noise, 1 kHz, typ, nV/$\sqrt{\text{Hz}}$	4.7 (4.7)	4.7 (4.7)	17 (max)	15 (max)
0.1 to 10 Hz, typ, μVp-p	0.12 (0.12)	0.12 (0.12)	3.3 max	2.5 max
Current noise, 1 kHz, max, fA/$\sqrt{\text{Hz}}$	400 (450)	400 (450)	0.6	0.6
Bias current, nA, max, 25°C	600 (650)	600 (650)	2 pA	1 pA
max over temperature	700 (750)	700 (750)	23 pA typ	23 pA typ
Offset current, nA, max over T	50 (50)	50 (50)	2 pA typ	2 pA typ
CMR, dB, min over temperature	97 (90)	94 (87)	86	90
Gain-bandwidth product, MHz, typ	3.4 (3.5)	3.4 (3.5)	1.6	1.6
Slew rate, V/μs, 2 kΩ load, typ	1.2 (0.9)	[0.8 (0.6)] min	1	1
Settling time to 0.01% [0.1%], μs typ	[9 (5.8)]	[9 (5.8)]	11 (10)	11 (10)
Open-loop gain, min over T (2 kΩ)	2 (2) V/μV	2 (2) V/μV	100 dB	100 dB
Output current, mA min	±7 (+6.7)	±7 (+6.7)	±5	±5
Short-circuit, mA typ	±40 (30)	±40 (30)	±15	±15
Supply current, mA, max over temp	5 (4)	5 (4)	1.5	1.5
Price, $US (1000s, DIP or SOIC)	(DIP) $4.97	(DIP) $2.21	$2.35	(DIP) $3.16

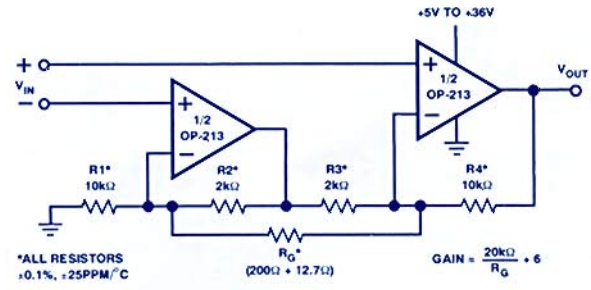


Figure 1. Ultra-low-noise single-supply instrumentation amplifier.

The **AD795**, a low-noise precision FET-input operational amplifier, offers the very low bias current of a FET-input device and the low voltage noise and offset drift of a bipolar-input op amp. Its 10^{14}-Ω common-mode impedance insures that the input bias current is essentially independent of common-mode and supply-voltage variations.

It has excellent dc specs, plus guaranteed and tested maximum input voltage noise. The K version guarantees 1 pA maximum input bias current and 250 μV maximum offset voltage; and the AD795 draws only 1.5 mA of supply current. The low bias current permits current measurements from such sources as low-noise photodiodes. The combination of low offset voltage & drift (3 μV/°C), low bias current, and high common-mode impedance makes it ideal for non-loading low-voltage measurements from high-impedance sources. For example, Figure 2 illustrates its application as a temperature-correcting† pH probe amplifier with an output voltage of 1 volt per pH unit.

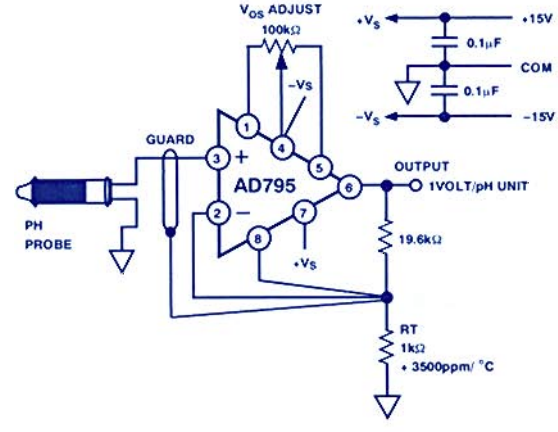


Figure 2. A pH probe amplifier.

At present, J and K versions are available in plastic DIPs, for 0 to +70°C. The J version is also available in 8-pin SO, with a 3-pA maximum 25°C bias current specification.

The AD795 was designed at Wilmington MA by JoAnn Close; the OP-213 was designed at Santa Clara CA by Derek Bowers.

*Use the reply card for technical data. Circle 20 for OP-213, 21 for AD795

†The temperature-sensitive correction resistor, RT, is available from Tel Labs, Inc., 154 Harvey Road, P.O. Box 375, Londonderry NH 03053. Telephone (603) 625-8994.

Monolithic 80-dB +5-V Single-Supply Log Amp has 50-MHz Frequency Range

Low-power AD606 provides signal-strength indication for mobile phones and receivers. Includes high-performance limiter

The AD606* is a complete monolithic demodulating logarithmic amplifier with 80-dB dynamic range for applications at center frequencies up to 50 MHz. Operating from a single +5-volt supply, it consumes 65 mW (325 μW when powered down).

Designed as a demodulating logarithmic amplifier for received-signal-strength-indicator (RSSI) functions in mobile phones and receivers, the AD606 is also effective as a high-performance limiting amplifier in FM demodulators and wireless local-area-network equipment. Featuring a 9-stage successive-detection architecture (like the AD640*—*Analog Dialogue* 23-3, 1989, pp. 3-6), it provides both log and limited outputs (Figure 1). Unlike alternative solutions requiring multiple single-stage ICs or transistor arrays and diodes, the monolithic AD606 provides superior performance and wider frequency range at lower cost.

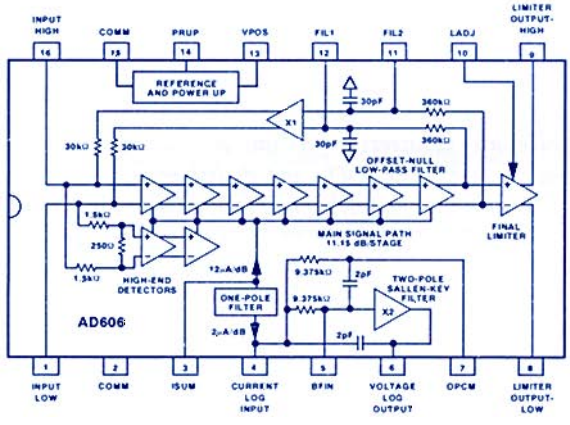


Figure 1. Block diagram of the AD606.

As a **log amp** (Figure 2), its overall dynamic range is −75 to +5 dBm (dB above 1 mW in 50 Ω), with log conformance flat to within ±1.5-dB max (±0.4 dB typical). The 37.5-mV/dB scaling provides a 3-volt output range, +0.5 V to +3.5 V, corresponding to the specified input range. Input noise is 1.5 nV/$\sqrt{\text{Hz}}$ maximum. The chip includes 3-pole filter circuitry following the demodulator.

As a **limiter**, the AD606 provides a hard-limited signal output as an adjustable differential current of ±1.2 mA full-scale from open-collector outputs, with flatness typically better than ±1 dB maintained over the 80-dB specified input range. The limiter can maintain ±3° phase stability at 10.7 MHz over the 80-dB range.

The device operates on a single +5-volt supply, with 65-mW typical power consumption. A CMOS-compatible standby-mode-control signal reduces power consumption to less than 1 mW

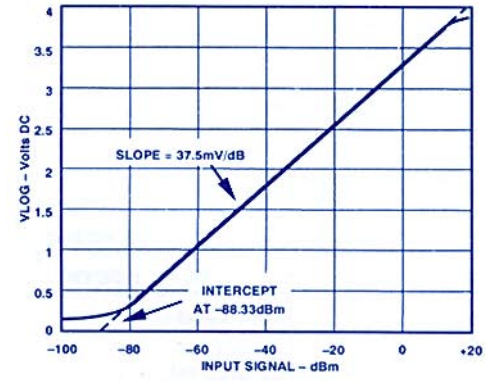


Figure 2. Logarithmic transfer function, V_{LOG} vs. input signal level.

within 5 μs; recovery to full functionality takes only 3.5 μs. The device is specified for 0 to +70°C operation and is available as a 16-pin plastic DIP or narrow-body SOIC for max performance in small space. Price in either package is $19.95 in 1000s.

APPLICATIONS

Here are some ways in which the AD606 is useful:

- *Cellular* phones continually measure their received rf power in order to predict the minimum power they must transmit to maintain the link back to the cell base station (to minimize battery power and adjacent-channel interference).
- *FM receivers* for satellite transmission: the AD606 provides excellent performance as a limiter at IFs up to 70 MHz.
- *Wireless local-area networks* (LANs) must cope with about 80 dB of signal variation due to attenuation and fading; they require good "video-response" time to avoid data corruption.
- *RF instrumentation* uses log amplifiers to measure the amplitude of wide-dynamic-range, wideband signals.
- *Ultrasound imaging* equipment uses log amps to extend the effective dynamic range of A/D conversion.

Figure 3 shows how the AD606 is connected for a basic RSSI application (the calibration adjustments could be omitted in non-critical applications). Typical measurement applications are as the log/IF strip in a spectrum- or network analyzer, or—adding an FM or QPSK demodulator, fed by the limiter outputs—as an IF strip in a GSM digital mobile radio or FM receiver.

The AD606 was designed by Barrie Gilbert at Analog Devices' Northwest Labs, Beaverton, Oregon.

*Use the reply card for technical data. Circle 22 for AD606, 23 for AD640

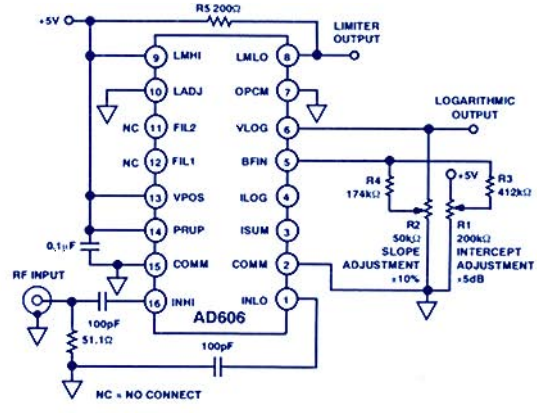


Figure 3. AD606 applied to indicate receiver signal strength.

Complete 12-Bit 10- and 25.6 MSPS A/D Converters

Monolithic AD872 converts at 10 MSPS; Hybrid AD9032 converts at 25.6 MSPS, has 74-dB SFDR, 150-MHz BW

The AD872 and AD9032 represent the best in available monolithic and hybrid 12-bit high-performance high-speed A/D converter technology for today's marketplace. Both devices are complete, including references, track/hold, and a/d converter. The monolithic AD872 provides 10-MSPS performance in a small package at low dissipation and lowest cost, and the AD9032 provides previously unavailable performance at 25.6-MSPS sampling rates. Evaluation boards are available for both devices.

The AD872 (Figure 1) is a complete and ready-to-go TTL/CMOS 12-bit, 10-MSPS A/D converter that requires 1/3 the power, 1/6 the board space, and half the cost of hybrids that perform a similar function. It includes an on-chip differential-input track-and-bold amplifier (eliminating the need for buffer circuitry) and a 2.5-volt reference. The reference source can furnish 2 mA to external destinations; thus, the AD872 can also serve as a precision system reference. The entire device dissipates only 1.15 watts and is available in a 28-pin DIP or a 44-pin LCC.

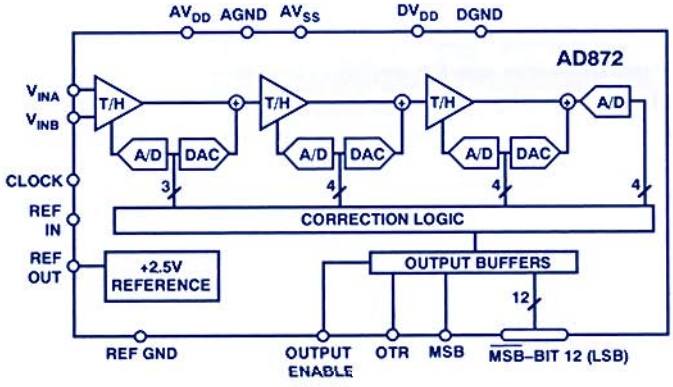


Figure 1. AD872 block diagram.

Table 1. Comparing the specifications (over temperature)

	AD872JD	AD9032A	AD9032B
Integral nonlinearity, LSB, typ	±2.5	2.0	2.0
Differential nonlinearity, LSB	±0.5 typ	1.75 max	1.5 max
No-missing codes-guaranteed	12 bits	12 bits	12 bits
Max encode rate, MSPS, min	10	25.6	25.6
Analog bandwidth, MHz	70 typ	150 min	150 min
Signal-to-noise and distortion			
dB, min at 1.2(1.0) MHz	(61)	61	63
dB, typ at 4.99 MHz	63		
dB, min at 9.6 MHz		60	61
Harmonic distortion			
dB, max at (1.0)1.2 MHz	(−63) THD	−67	−70
dB, typ at 4.99 MHz	−66 THD		
dB, max at 9.6 MHz		−64	−68
Spurious-free dynamic range	70 dB	74 dB (12 MHz)	74 dB (12 MHz)
Aperture jitter, ps rms, max	10 typ	8	8
Power dissipation, W, max	1.25	4.5	4.5
Price, 100s, $US	$165	$950	$1100

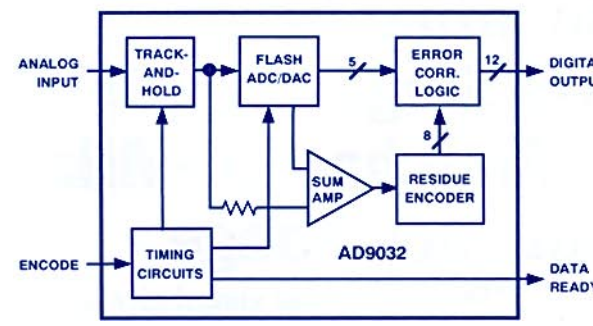


Figure 2. AD9032 block diagram.

The completeness-of-function is augmented with a full range of ac and dc parameters guaranteed over the full operating temperature range: signal to noise-plus-distortion (S/N+D) at 1 MHz is 65 dB; differential nonlinearity is typically only 0.5 LSB, and no missing codes are guaranteed for the full 12-bit resolution. The AD872's performance is well-suited to high-resolution imaging systems, such as film scanners and infra-red imagers, as well as high-speed data acquisition for radar, instrumentation, and communications.

The AD872 is available in J (0 to +70°C) and S (−55 to +125°C) grades. S versions fully qualify under MIL-STD-883 level B, and a standard military drawing is pending DESC approval. The AD872 operates from ±5-volt supplies.

The AD9032 (Figure 2) is a complete ECL-compatible 12-bit, 25-MSPS ADC, including track-and-hold, encoder, references, and timing; it is pin-compatible with the 20-MSPS AD9034 (*Analog Dialogue* 26-1, 1992), but uses less power. It is well-suited to all sampling applications requiring a broad dynamic range over a wide analog bandwidth—for use in such equipment as digital scopes, waveform digitizers, spectrum analysis, medical ultrasound imaging, radar, SIGINT, and digital receivers. Figure 3 shows a typical output spectrum for a 12.1-MHz sinusoidal signal, sampled at 25.6 MSPS. The AD9032 is available for −25 to +85°C and −55 to +125°C temperature ranges and is housed in a 40-pin ceramic DIP or leaded flatpack.

The AD872 was designed at Wilmington MA by Dave Robertson, and the AD9032 was designed in Greensboro NC by Keith Lanier.

*For technical; data use the reply card. Circle 24 for AD872, 25 for AD9032

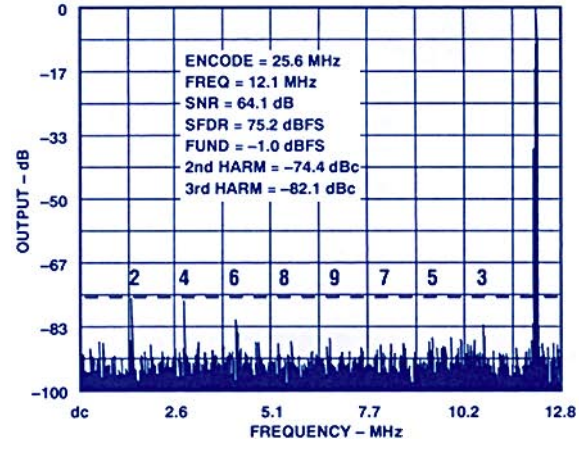


Figure 3. Typical AD9032 spectrum, 12.1-MHz input.

What's New in DSP

- **Low-Cost Processors**
- **Faster Floating Point**
- **New EZ-Tools**
- **More Partnerships**

*We've received a whole lot of important information and news about DSP and mixed-signal products. To ensure its timeliness (if not completeness), it will be succinctly summarized on this page. For further details on specific items, use the reply card. To be sure of receiving DSP updates regularly, with considerably greater detail, you are invited to subscribe to our sister publication, "DSPatch, the Digital Signal Processing Applications Newsletter."**

NEW AND IMPROVED PROCESSORS

The **ADSP-2115**† is a low-cost, high-performance DSP, combining features of the **ADSP-2101** with a cost closer to that of **ADSP-2105**. Pin- and code-compatible with both devices, it gives the user a simple path to increased performance from the ADSP-2105—or to cost reduction from the ADSP-2101.

The ADSP-2115 combines the 16-bit fixed-point ADSP-21xx core processor with 1K words of program RAM, 512 words of data RAM, two serial ports, boot circuitry, and an interval timer in a 68-lead PLCC or 80-lead PQFP. It is available in three speed grades: 10.24, 13.824, and 16.67 MHz. The 13.824-MHz clock speed is the same as that of the AD28msp01 modem front end or the AD28msp02 voice front end, for ease of use in Signal Computing chip-sets.

If you haven't looked lately, the **ADSP-2111** (used in such applications as the Olivetti *Quaderno* notebook PC and the Siemens Neural-Net Speech Recognizer for mobile telephones) is now available at lower prices. Consult the nearest distributor or Analog Devices. The ADSP-2111 features a host interface port and bidirectional, double-buffered serial ports.

The **ADSP-21020** floating-point DSP is now available for 33.3-MIPS instruction rate (30-ns cycle time—single-cycle execution); ask for ADSP-21020KG-133†. Benchmarks include: 1024-point complex FFT, 0.58 ms; divide (y/x), 180 ns; inverse square root ($1/\sqrt{x}$), 270 ns.

Three fully qualified **military** versions of the floating-point **ADSP-21020**† are available, for 20, 25, and 30 MIPS. For those military applications involving Ada, Meridian Software Systems (a subsidiary of Verdix Corp.) is working to port their Ada compiler to the ADSP-21020. A fast, efficient, complete compiler, validated by the Ada Joint Program Office, it supports pragma interfaces for C and assembly languages and includes utilities for automating software development, managing libraries, and debugging.

NEW TOOL PACKAGES

ADSP-2111 EZ-KIT, now available, is the lowest-cost, best-value DSP development kit on the market. It includes software development tools for IBM-PC compatibles, the ADSP-2111 Simulator, the ADSP-2111 EZ-LAB® Evaluation Board, and *support*—books, sample applications on diskette, and a worldwide staff of trained application engineers. Ask for ADDS-2111-EZ-KIT. Price: $499.

Analog Devices EZ-Tools now include an EZ-LAB Evaluation Board and EZ-ICE® In-Circuit Emulator for the **ADSP-21msp50** mixed-signal processor (processor + on-chip A/D and D/A converters) to support prototyping, development, and debugging. With EZ-ICE, one can test and debug one's application on the mixed-signal processor without making a major financial commitment. Ask for ADDS-21msp50-EZ-LAB and -EZ-ICE.

EZ tools for the floating-point **ADSP-21000** family are also available: EZ-LAB Evaluation Board (pre-programmed demos or programs downloaded from a PC), EZ-ICE In-Circuit Emulator (uses JTAG port to observe, debug, test, and monitor), EZ-KIT, and EZ-KIT Plus with C compiler. Ask for ADDS-21020/21010 EZ-Tools.

NEWS

- Analog Devices and Spectron Microsystems, Inc., have signed an agreement to port Spectron's **SPOX DSP Operating System™** to the ADSP-21000 floating-point DSP family. With SPOX, programmers no longer need to develop and debug their own multitasking, real-time operating system; multiple real-time applications can be run concurrently. In addition, the high-level support provided by SPOX means that, with minimal effort, existing programs can be ported to the DSP family offering the best price and performance. [FAX requests for information to Applications Engineering at (617) 461-3010]

- Another **Signal-Computing** application: For **digital telephone answering machines** (DTAM), and other voice-record-and-playback systems, Analog Devices is now beta-testing a solution in the form of the ADDS-CSDK-100 **Compressed Speech Design Kit** and the ADSP-2106-CSDK100, a ROM-coded ADSP-2105 coded to run an RPE-LPC (GSM) speech algorithm licensed from Digianswer. For information, phone DSP Marketing at (617) 461-3881.

- MIT/Lincoln Laboratory has selected Analog Devices, Electronic Designs, Inc., and Westinghouse Electronic Systems Group to develop a high-performance DSP chip. The **single-chip DSP—based on the ADSP-21020 floating-point core with 100 MFLOPS performance**—is intended initially for high-performance radar and IR applications, image analysis, missile guidance, FIR filtering, and high-performance graphics.

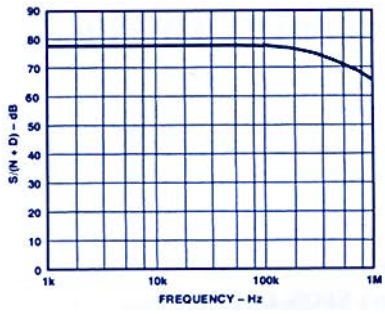
The CMOS DSP devices will advance VLSI process technology with 0.6-micron geometry and 3.3-volt operation, and will lead to commercial parts for the open market. Westinghouse is managing the program and providing radar and electronic system expertise; and Electronic Designs is implementing the large on-chip SRAM memory. Devices will be delivered late this year for building multiprocessing systems, such as a 64-processor array with 6.4-GFLOPS peak performance—a low-power "massively parallel" system requiring little if any "glue" logic. The outlook for DSP in 1994 is indeed exciting.

*For a subscription to *DSPatch* and a copy of the latest issue, use the reply card. Circle 35

†For information on these products, use the reply card. Circle 26 for ADSP-2115, 27 for ADSP-2101 and 28 for ADSP-2105, 29 for AD28msp01, 30 for AD28msp02, 31 for update on ADSP-21020 family and its EZ tools, 32 for ADSP-2111 and its EZ-KIT, 33 for ADDS-21msp50 EZ-LAB & EZ-ICE, 34 for military version of ADSP-21020.

Fast Sample-Hold

Low power & cost, 250-ns acquisition time



The **AD783*** is a complete sample-hold amplifier for very-high-speed applications requiring up-to-12-bit performance. Designed for use with high-speed A/D converters (such as the AD671, AD7586, AD674B, AD774B, AD7572, and AD7672), it is complete—including the *hold* capacitor, requires no external components, is easy to use, and is fully specified in the time and frequency domains. Housed in space-saving 8-pin Cerdip and SOIC packages, it is available at a money-saving price. ($12.00 in 100s)

The AD783 has a 250-ns typical acquisition time (375 ns max) to 0.01%, low aperture jitter (20 ps typical) and low *hold*-mode harmonic distortion (−80 dB max). Besides being an excellent fit with high-speed ADCs, its 15-MHz typical small-signal bandwidth is useful in undersampled systems, such as digital radio. Other applications include sampling the output pixel streams of linear CCDs and infrared focal-plane arrays.

A patented architecture featuring self-correction minimizes hold-mode errors and ensures specified accuracy over the full commercial (J grade, 0 to +70°C) and extended industrial (A grade, −40 to +85°C) temperature ranges (a MIL-temp /883 version is scheduled to be available in spring, 1993).

The AD783's dynamic performance enhances system accuracy, with maximum hold-mode offset of 5 mV and droop of 1 μV/μs (0.02 μV/μs typical). Operating from ±5-volt supplies, the AD783's 95-mW typical power consumption, 1/3 that of comparable devices, makes it an excellent choice for portable- or battery-powered equipment. ▶

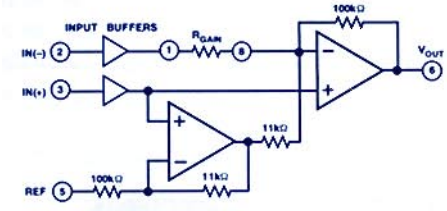
*Use the reply card for data. Circle 36

Precision Single-Supply In Amp

AMP-04 has 1-to-1000 single-resistor gain range Plus low offset voltage, supply current, and price

The AMP-04† precision single-supply instrumentation amplifier amplifies the difference between a pair of input voltages while rejecting common-mode noise and offsets. Designed to work with supply voltages from +5 V to ±15 V, it combines accuracy, low power consumption, wide input-voltage range, and excellent gain performance.

With a +5-volt supply, the low-power AMP-04 draws a maximum supply current of 850 μA (over temperature). It accepts input signals from 0 to +3 volts with an output range from zero (within 2 mV max, E version) to +4.0 V. Thus it produces zero-volts-out-for zero-volts-in. A Reference input provides for a pseudo ground in applications where the difference may be of either polarity. Input offset (E version) is less than 300 μV over temperature, with a maximum drift rate of 30 μV/°C; the output offset is a maximum 3 mV over temperature.



The inputs are buffered and at high impedance (typically 4 GΩ dynamically), with bias current of only 50 nA over temperature. Common-mode rejection at a gain of 1000 is 90 dB minimum, 85 dB min over temperature. The gain equation, $G = 100\ k\Omega/R_{GAIN}$, is accurate to within 0.5% max (0.8% over temperature), and nonlinearity at G = 100 is only 0.025%. Small-signal bandwidth is typically 300 kHz

The AMP-04 is available in two grades, E and F, packaged in 8-lead plastic DIP and SOIC. Prices (1000s) start at $4.55. ▶

†Use the reply card for technical data. Circle 37

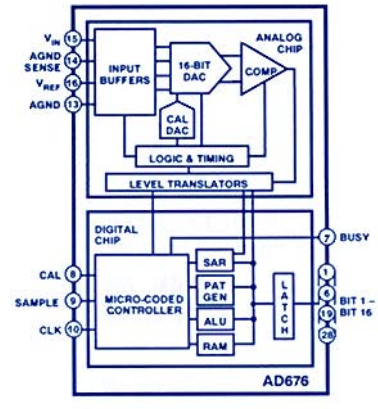
16-Bit, 100-kSPS Sampling ADC

AD676 is autocalibrated, has ac & dc specs, ±1.5-LSB max integral nonlinearity over temperature

The AD676§ is a high-performance 16-bit sampling A/D converter with parallel output housed in a 28-pin side-brazed ceramic DIP. It converts at speeds up to 100 ksps and has a full-power signal bandwidth of 1 MHz. An autocalibrating device, it digitally corrects for internal nonlinearities. Using the system's voltage reference, it provides high accuracy without trimming.

A general-purpose device, it is characterized for both dc and dynamic performance. Its specifications include 16-bit performance with no missing codes over temperature, ±1.5-LSB max integral nonlinearity and 87-dB min S/(N+D) over temperature (B version, 83-ksps sampling). Total harmonic distortion is −90 dB max over temperature at 83 ksps, and typically −92 dB over temperature at 100-ksps. Typical applications include signal processing, for imaging and communications, and measurement systems.

The AD676 has two chips (compound monolithic integration), operates from



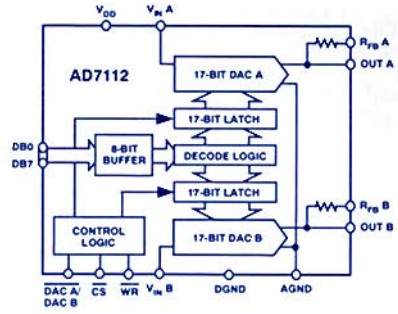
±12-V and +5-volt supplies and typically consumes 360 mW during conversion. Ground sensing is included for the analog input, and separate analog and digital grounds are provided. Two grades apiece (J,K and A,B) are provided for the commercial and industrial temperature ranges. Prices start at $39 in 100s. ▶

§Use the reply card. Circle 38

LOGDACs: 88.5-dB Gain Range

AD7111A & AD7112 for single-channel & stereo: 0.375 dB-per-step precision digital gain control

A LOGDAC® is a low-distortion multiplying digital-to-analog converter; each 1-bit change of digital input produces a fixed ratio of gain change (see *Analog Dialogue* 16-2, 1982, p. 18). For the **AD7111A** single* & **AD7112** dual* LOGDAC, the attenuation change per bit is 0.375 dB (or a ratio of 1/1.044), from 0 dB (unity gain) down to a maximum specified attenuation of 88.5 dB (1/26,600).



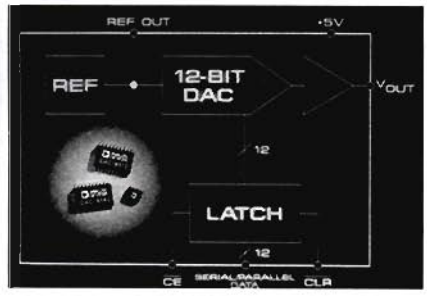
AD7111A/AD7112 are available in 16/20-pin DIPs and SOICs and are broadly applicable for digital gain setting in any phase of professional, consumer, or automotive audio. Although voltage-controlled amplifiers (VCAs) may cost less, they cannot match the low distortion of these devices (−91-dB THD at 1 kHz @ 6 V rms, using an AD711 or dual AD712 op amp as output amplifier) or their ability to work under digital control, with on-chip latches and control logic. Prices start at $4.15/$5.60 in 1000s.

Besides the op amp, the AD7111A/AD7112 require a single +5-volt supply for excitation and a 3-wire µP or DSP interface for control. They can be set to accept data in 25 ns; and the 57-ns *write* pulsewidth is compatible with standard µPs. An 8-bit parallel word, written to the data latch, establishes the attenuation of each DAC channel. They can also be connected in the amplifier feedback path for stepped *gain*, instead of attenuation.

*Use the reply card for technical data. For AD7111A circle 39; for AD7112 circle 40

12-Bit DACPORTs

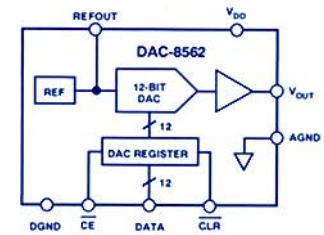
Single-supply, complete Serial & parallel, 3 mW



The DAC-8512‡ and DAC-8562‡ DACPORTs® are complete, voltage-output 12-bit digital-to-analog converters designed to operate on a single +5-volt supply. The DSP-compatible **DAC-8512,** loaded serially, is housed in mini-DIP and low-profile 1.5-mm-height(!) SO-8 packages; the parallel-loading DAC-8562 uses 20-pin DIPs & SOICs. Both are complete—with 12-bit voltage-switched DAC, internal 2.5-volt laser-trimmed reference, and output amplifier.

Besides being housed in packages with a very small footprint, these devices have low dissipation (3 mW typical, 5 mW max in low state)—ideal for battery-operated systems. While operating on a single +5-volt supply, the output amplifier can swing rail to rail. However, it is scaled for easy programming, 1 mV per bit (0 to 4.095 V).

The DAC-8512 and DAC-8562 are designed for anyone with a 12-bit requirement who is designing portable equipment or needs to save space. Other features to think about include: no external components required, ±5-mA output current, extended industrial temperature range (−40 to +85°C), low zero- and full-scale errors (max over temperature 3 mV and 6 mV). Two performance grades are available, E and F. Prices start at $6.95 (100s)

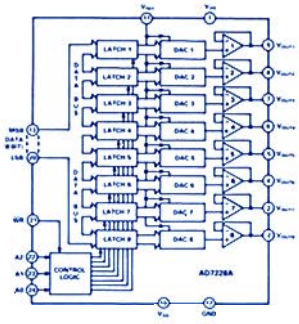


‡Use the reply card. Circle 42 for DAC-8512; 43 for DAC-8562

Octuple 8-Bit Voltage-Output DAC

Improved AD7228A operates on +5-V supply Specified for −40 to +85°C, with lower price

The AD7228A† is a new and improved version of the AD7228 octuple 8-bit voltage-output DAC, the first of its kind, introduced in these pages in 1987 (*Analog Dialogue* 21-2). The AD7228A, considerably faster than competitive devices, is specified for operation with +5-volt single supply as well as with dual supplies. Packages include narrow 24-pin DIP and SOIC, and 28-pin PLCC. Prices start at $17.25 in 100s, $14.65 in 1000s.



Principal applications for multiple 8-bit DACs are in producing multi-channel digitally programmed fixed- or variable voltages for such applications as pin-drivers in automatic test equipment (ATE) and set-points in automatic control.

The voltage-output AD7228A has eight output amplifiers, and requires just a single reference voltage: 1.25 V for single-supply +5-V operation, and from 2.0 to 10 V for dual supply operation with V_{DD} from 10.8 to 16.5 volts.

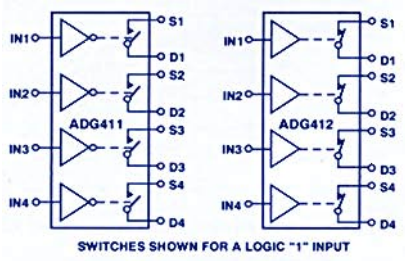
The AD7228A is available in B & C grades for the extended industrial temperature range (−40 to +85°C) and a variety of packages, as noted above. Relative accuracy with +5-V supplies is ±2 LSBs, all grades.

†Use the reply card. Circle 41

Quad SPSTs

Handle signals to rails

ADG411/412: low R_{ON}

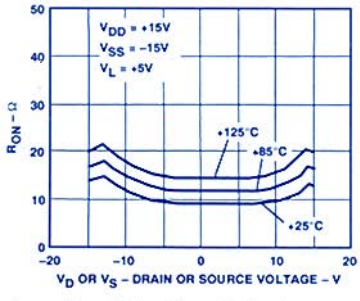


The ADG411 and ADG412* contain four independently selectable single-pole, single-throw (SPST) analog switches. They differ only in control polarity: switches are closed by logic 0 in ADG411, logic 1 in ADG412. They provide improved performance in all applications for '411 and '412-type switches.

A trench-isolated linear-compatible CMOS process (LC^2MOS) provides latchup-proofing and low leakage. Breakdown voltage is high (44 V), and the switches can operate with signal voltages that extend to the supply rails. *On*-resistance is low (45 Ω max) and switching is fast (t_{ON} 175 ns max and t_{OFF} 145 ns max) over temperature (vs. 25°C specs for competitive devices); all specs are valid for a 10% supply-voltage tolerance.

The switches' flat on-resistance profile provides good linearity and low distortion (−93 dB) in audio applications. The fast switching and > 40-MHz signal bandwidth make them useful in video switching. Other applications include communications, test, data acquisition, and portable equipment.

The devices are specified for both dual- (±15 V) and single-supply (+12 V) operation. The B grade is available for −40 to +85°C, packaged in DIPs and SOICs. A T grade will also be available for −55 to +125°C. Prices start at $2.30 in 1000s.



*Use the reply card for data. Circle 44

200-MHz Pin Driver for ATE

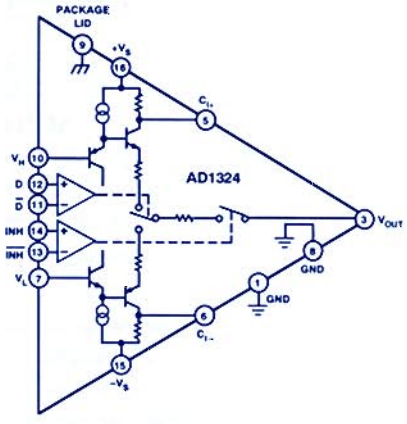
For VLSI and memory test: ECL, TTL & CMOS

AD1324 has 2-V/ns slew rate, 200-ps edge match

The AD1324† is a monolithic pin driver circuit used in test equipment for VLSI- and memory circuits to provide precisely controlled transitions between logic high and -low levels in operation at speeds up to 200 MHz. A lower-cost alternative to "in-house" designs, its guaranteed maximum specifications include 250-ps edge matching, 2-ns rise and fall time for 3-V input swings (6.5 ns for 9-V input swings), and 15-ns settling time for inputs between 1 and 7 V. Programmable outputs range from −2 V to +7 V, with maximum output swings from 100 mV to 9 V.

The device switches to the high-impedance *inhibit* mode within 1.3 ns (1.6 max), disconnecting the device-under-test from the drive signal and avoiding long system delays associated with waiting for loads to clear. Both data and inhibit circuits have differential inputs.

Packaging is a critical factor in ATE pin-electronics design. Component size and cost of the electrical interface between the system and the device under test must be minimized. The AD1324 is housed in an ultra-small 16-lead hermetically sealed surface-mount package. It is specified for operation from 0 to +70°C and dissipates 900 mW. Price begins at $85 in 100s.



†Use the reply card for technical data. Circle 45

100-MHz Direct Digital Synthesizer

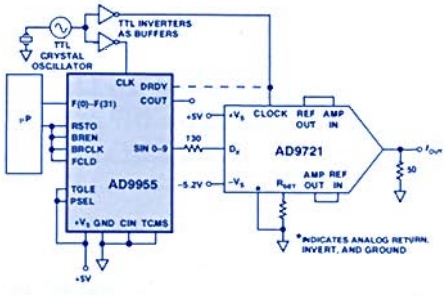
AD9955 phase accumulator-12-bit sine converter

Continuous frequency update, >90-dB SFDR

The AD9955‡ is a monolithic CMOS direct digital synthesizer, comprising a 32-bit phase accumulator and a 15-bit-phase-to-12-bit-sine amplitude conversion circuit. It generates a sampled digital sine wave, which—applied to a fast D/A converter, such as the AD9721 or AD9713B—produces an analog sine wave at a digitally controllable frequency. The figure shows an application with the 10-bit AD9721.

The phase accumulator is a digital circuit which generates the phase increment of the output waveform, based on the clock frequency and a digital Δ-phase input: $f_{OUT} = f_{CLOCK}\ (\Delta phase/2^N)$. In effect, the accumulator serves as a variable-frequency oscillator generating a digital ramp, which is then converted to a digital sine.

The AD9955 will typically handle clock rates up to 100 MHz (85 MHz min), and its output has a spurious-free dynamic range (SFDR) in excess of 90 dB. Frequency can be updated continuously, and available output is signalled by a Data-Ready signal. Typical applications include frequency synthesizers, digital demodulation, FM modulators.



The AD9955 is available in an 80-lead plastic quad flatpack (PQFP) for commercial temperature-range (0 to +70°C) applications. An evaluation board is available. Prices start at $29 in 100s for the AD9955, $349 for the evaluation board.

‡Use the reply card. Circle 46

Ask the Applications Engineer—13

CONFUSED ABOUT AMPLIFIER DISTORTION SPECS?

by Walt Kester

Q. *I've been looking at your amplifier data sheets and am confused about distortion specifications. Some amplifiers are specified in terms of second- and third-harmonic distortion, others in terms of* total harmonic distortion (*THD*) *or* total harmonic distortion plus noise (*THD+N*), *still others have some of these specifications as* well as two-tone intermodulation distortion *and* third-order intercept. *Can you please clarify?*

A. Because the amplifier is fundamental to a wide range of uses, it is natural that many application-specific specifications have evolved as new amplifiers have been developed to meet those needs. So—as you so rightly pointed out—distortion may be specified in various ways; the spec depends on how distortion is defined by users for the particular application. Some distortion specifications are fairly universal, while others are primarily associated with specific frequency ranges and applications.

But there is some standardization of the basic definitions, so let's talk about them first. Harmonic distortion is measured by applying a spectrally pure sine wave to an amplifier in a defined circuit configuration and observing the output spectrum. The amount of distortion present in the output is usually a function of several parameters: the small- and large-signal nonlinearity of the amplifier being tested, the amplitude and frequency of the input signal, the load applied to the output of the amplifier, the amplifier's power supply voltage, printed-circuit-board layout, grounding, power supply decoupling, etc. So you can see that any distortion specification is relatively meaningless unless the exact test conditions are specified.

Harmonic distortion may be measured by looking at the output spectrum on a spectrum analyzer and observing the values of the second, third, fourth, etc., harmonics with respect to the amplitude of the fundamental signal. The value is usually expressed as a ratio in %, ppm, dB, or dBc. For instance, 0.0015% distortion corresponds to 15 ppm, or −96.5 dBc. The unit "dBc" simply means that the harmonic's level is so many dB below the value of the "carrier" frequency, i.e., the fundamental.

Harmonic distortion may be expressed individually for each component (usually only the second and third are specified), or they all may be combined in a root-sum-square (RSS) fashion to give the *total harmonic distortion* (THD).

$$THD = \frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + \ldots + V_n^2}}{V_s}$$

where

V_s = signal amplitude (rms volts)
V_2 = second harmonic amplitude (rms volts)
V_n = nth harmonic amplitude (rms volts)

The number of harmonics included in the THD measurement may vary, but usually the first five are enough. You see, the RSS process causes the higher-order terms to have negligible effect on the THD, if they are 3 to 5 times smaller than the largest harmonic[$\sqrt{0.10^2+0.03^2} = \sqrt{0.0109} = 0.10 \approx 0.10$].

The expression for THD+N is similar; simply add the noise in root-sum-square fashion (V_{noise} = rms value of noise voltage over the measurement bandwidth).

$$THD+N = \frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + \ldots + V_n^2 + V_{noise}^2}}{V_s}$$

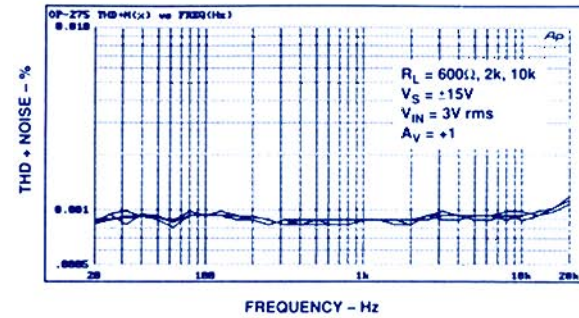
It should be evident that THD+N ≈ THD if the rms noise over the measurement bandwidth is several times less than the THD, or even the worst harmonic. It is worth noting that if you know only the THD, you can calculate THD+N fairly accurately using the amplifier's voltage- and current-noise specifics. (Thermal noise associated with the source resistance and the feedback network may also need to be computed). But if your rms noise level is significantly higher than the level of the harmonics, and you are only given the THD+N specification, you cannot compute the THD.

Special equipment is often used in audio applications for a more-sensitive measurement of the noise and distortion. This is done by first using a bandstop filter to remove the fundamental signal. The total rms value of all the other frequency components (harmonics and noise) is then measured over an appropriate bandwidth. The ratio to the fundamental is the THD+N spec.

Q. *How are the distortion specs looked at over the various frequency ranges and applications?*

A. I think the best way is to start at the low frequency end of the spectrum and work our way up; that will make it easier to see the underlying method.

Audio-frequency amplifiers are a good place to start. Types used here (such as the OP-275*) are optimized for low noise and low distortion within the audio bandwidth (20 Hz to 20 kHz). In audio applications, total harmonic distortion plus noise (THD+N) is usually measured with specialized equipment such as the Audio Precision System One. The output signal amplitude is measured at a given frequency (e.g., 1 kHz); then, as above, the fundamental signal is removed with a bandstop filter and the system measures the rms value of the remaining frequency components, which contain both harmonics and noise. The noise and harmonics are measured over a bandwidth that will catch the highest harmonics, usually about 100 kHz. The measurement is swept over the frequency range for various conditions. THD+N results for OP-275 are plotted here as a function of frequency.

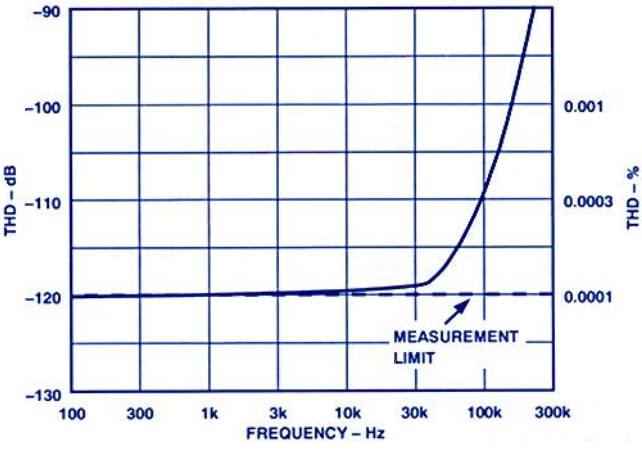


*Use the reply card for technical data. Circle 47

The signal level is 3 V rms, and the amplifier is connected as a unity-gain follower. Notice that a THD+N value of 0.0008% corresponds to 8 ppm, or −102 dBc. The input voltage noise of the OP-275 is typically 6 nV/$\sqrt{\text{Hz}}$ @ 1 kHz and, integrated over a 100-kHz bandwidth, yields an rms noise level of 1.9 μV rms. For a 3-V rms signal level, the corresponding signal-to-noise ratio is 124 dB. Because the THD is considerably greater than the noise level, the THD component is the primary contributor.

Q. *I noticed that Analog Devices recently introduced another low-noise, low-distortion amplifier (AD797) and that it is specified in THD, not THD+N. The actual specification quoted at 20 kHz is −120 dB. What gives?*

A. Actually, we are not trying to be misleading here. The distortion is at the limits of measurement of the available equipment, and the noise is even lower—by 20 dB! Here is the measured THD of the AD797* as a function of frequency.

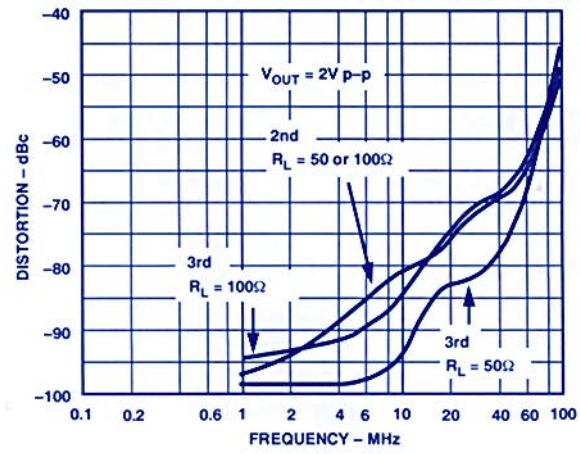


The measurement was made with a spectrum analyzer by first filtering out the fundamental sine-wave frequency ahead of the analyzer. This is to prevent overdrive distortion in the spectrum analyzer. The first five harmonics were then measured and combined in a root-sum-square fashion to get the THD figure. The legend on the graph indicates that the measurement-equipment "floor" is about −120 dB; hence at frequencies below 10 kHz, the THD may be even less.

For noise, multiply the voltage noise spectral density of the AD797 (1 nV/$\sqrt{\text{Hz}}$) by the square root of the measurement bandwidth to yield the device's rms noise floor. For a 100-kHz bandwidth, the noise floor is 316 nV rms, corresponding to a signal-to-noise ratio of 140 dB for a 3-V rms output signal.

Q. *How is distortion specified for high frequency amplifiers?*

A. Because of the increasing need for wide dynamic range at high frequencies, most wideband amplifiers now have distortion specifications. The data sheet may give individual values for the second and third harmonic components, or it may give THD. If THD is specified, only the first few harmonics contribute significantly to the result. At high frequencies, it is often useful to show the individual distortion components separately rather than specifying THD. The AD9620† is a 600-MHz (typical −3-dB bandwidth) low distortion unity-gain buffer. Here are graphs of the AD9620's second and third harmonic distortion as a function of frequency for various loading conditions.



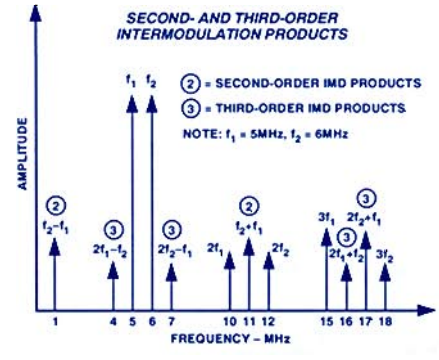
Q. *What are two-tone intermodulation products, and how do they differ from harmonic distortion?*

A. When two tones are applied to an amplifier that is non-linear, the nonlinearity causes them to modulate one another, producing intermodulation distortion (IMD) in the form of frequencies known as intermodulation products. (For the mathematical development of this concept, see Reference 1). For two tones at frequencies, f_1 and f_2 (where $f_2 > f_1$), the second- and third-order IM products occur at the following frequencies:

Second Order: $f_1 + f_2, f_2 - f_1$

Third Order: $2f_1 + f_2, 2f_2 + f_1, 2f_2 - f_1, 2f_1 - f_2$

If the two tones are fairly close together, the third-order IMD products at the difference frequencies, $2f_2 - f_1$ and $2f_1 - f_2$, may be especially troublesome because—as the figure shows—they are hard to filter out. Notice that the other second- and third-order IMD products—which occur at substantially higher or lower frequencies—can be filtered (if the only frequencies of interest are in the neighborhood of f_1 and f_2).



Two-tone intermodulation-distortion specifications are of especial interest in r-f applications and are a major concern in the design of communications receivers. IMD products can mask out small signals in the presence of larger ones. Although IMD has been rarely specified in op amps operating at frequencies less than 1 MHz, many of today's dc op amps are wideband types that can operate usefully at radio frequencies. For this reason, it is becoming common to see IMD specifications on fast op amps.

Q. *What are the second- and third-order intercept points, and what is their significance?*

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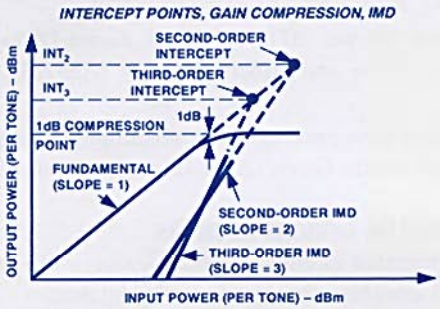
A. Usually associated with r-f applications, these specs provide figures of merit to characterize the IMD performance of the amplifier. The higher the intercept power, the higher the input level at which IMD becomes significant—and the lower the IMD at a given signal level.

Here's how it is derived: Two spectrally pure tones are applied to the amplifier. The output signal power in a single tone (in dBm) and the relative amplitudes of the second-order and third-order products (referenced to a single tone) are plotted (and extrapolated) here as a function of input signal power.



If you go through the mathematical analysis [1], you will find that if device nonlinearity can be modeled by a simple power-series expansion, the second-order IMD amplitudes tend to increase by 2 *dB* for every 1 dB of signal increase. Similarly, the third-order IMD amplitudes increase 3 *dB* for every 1 dB of signal increase. Starting with a low-level two-tone input signal and taking a few IMD data points, you can draw (and extrapolate) the second- and third-order IMD lines shown on the diagram.

Beyond a certain level, the output signal begins to soft-limit, or compress (coinciding with the increasing visibility of IMD products). If you extend the second- and third-order IMD lines, they will intersect the extension of the output/input line; these intersections are called the second- and third-order intercept points. The projected output power values corresponding to these intercepts are usually referenced to the output power of the amplifier in dBm.

Since the slope of the third-order IMD amplitudes is known (3 dB/dB), if the intercept is also known, the third-order products at any input (or output) level can be approximated. For a higher intercept, the line moves to the right (same slope), showing lower 3rd-order products for a given input level.

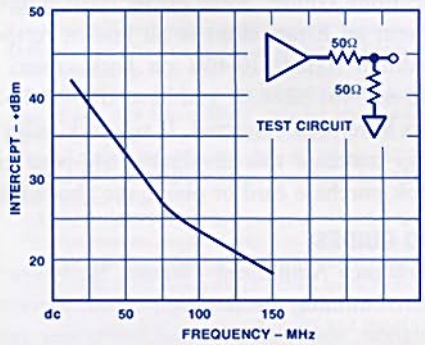
Many r-f mixers and "gain blocks" have 50-Ω input and output impedances. The output power is simply the power that the device transfers to a 50-Ω load. The output power is calculated by squaring the rms output voltage (V_o) and dividing by the load resistance, R_L. The power is converted into dBm as follows:

$$\text{Output power} = 10 \log_{10} \frac{\frac{V_o^2}{R_L}}{1\ \text{mW}}\ \text{dbm}$$

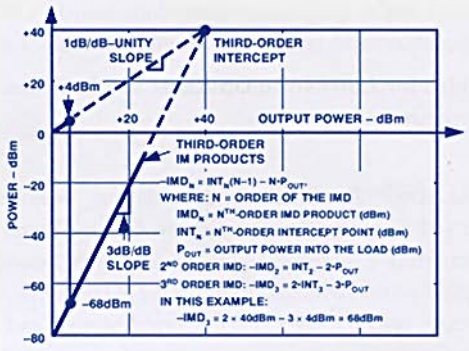
Since an op amp, on the other hand, is a low-output-impedance device, for most r-f applications, the output of the op amp must be source- and load-terminated. This means that the actual op amp output power has to be 3 dB higher than the power delivered to the load, as calculated from the above formula. In this type of application, it is customary to define the IMD products with respect to the *output power actually delivered into the 50-Ω load* rather than the actual op-amp output power.

Another parameter that may be of interest is the 1-dB compression point, shown in the figure. This is the point at which the output signal has started to limit and is attenuated by 1 dB from the ideal input/output transfer function.

The figure below is a plot of the third-order intercept power values for the AD9620 buffer amplifier as a function of input frequency. Its data can be used to approximate the actual value of the third order intermodulation products at various frequencies and signal levels.



Assume the op amp output signal is at 20 MHz with 2 V peak-to-peak into a 100-Ω load (50-Ω source and load terminations). The voltage into the 50-Ω load is therefore 1 volt peak-to-peak, with a power of 2.5 mW, corresponding to +4 dBm. The value of the third-order intercept at 20 MHz—from the graph—is +40 dBm. This permits a graphical solution, as shown below. For an output level of +4 dBm, the third-order IMD products, based on an extrapolation of the slope of 3 back from the intercept, amount to −68 dBm, or 72 dB below the signal.



This analysis assumes that the op-amp distortion can be modeled with a simple power series expansion as described in Reference 1. Unfortunately, op amps don't always follow simple models (especially at high frequencies), so the third-order intercept specification should primarily be used as a figure of merit, rather than a substitute for measurements.

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2. *High Speed Design Seminar*, 1990. Norwood, MA: Analog Devices, Inc. Use book purchase form.
3. *1992 Amplifier Applications Guide*. Norwood, MA: Analog Devices, Inc. Use book purchase form.

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MORE AUTHORS *(continued from page 2)*

Matt Smith (page 12) is a Senior Applications Engineer at our Limerick, Ireland, facility. His responsibilities include providing technical support for customers, writing data sheets and application notes, and defining new products. He holds a B.Eng. from the University of Limerick. His interests include windsurfing, paragliding, flying light aircraft, and playing squash.

Walt Jung (page 14) is a Corporate Staff Applications Engineer, working out of Fallston, MD. His photo and a biographical sketch appeared in *Analog Dialogue* 26-2.

Adolfo Garcia (page 14) is a Staff Applications Engineer for Analog Devices in Santa Clara, CA. His photo and a biographical sketch appeared in *Analog Dialogue* 26-1.

Walter Kester (page 27) is a Corporate Staff Applications Engineer for Analog Devices in Greensboro, NC. His photo and a biographical sketch appeared in *Analog Dialogue* 26-2.

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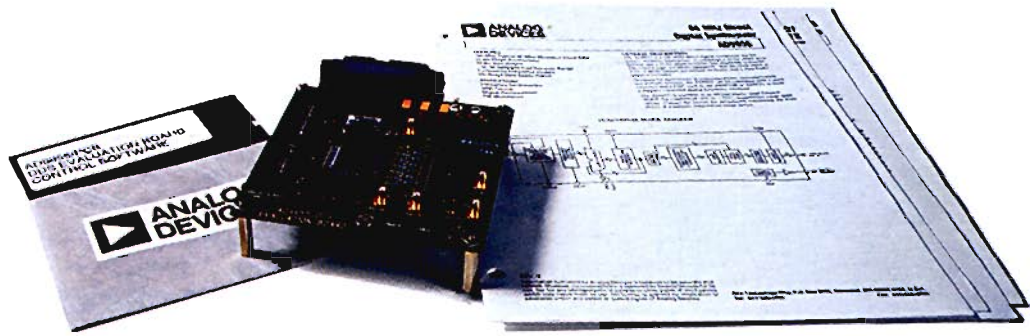

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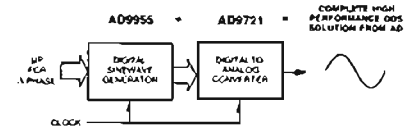

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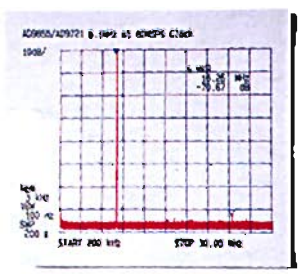

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